Department: Electrical and Computer Engineering

EEL 4710L — Introduction to Field Programmable Logic Devices Laboratory

Curriculum Designation: Elective lab for EE majors. Required laboratory for CpE majors.

Course (Catalog) Description: Laboratory in support of EEL 4710.

Prerequisite: EEL3705; EEL3705L
Corequisite: EEL 4710

Text and/or other required material: Online Lab manual

Course Objectives:

1. Design, implement, test, and debug a TCL/TK script to verify a VHDL design via simulation.
2. Demonstrate a basic understanding of IP catalogs and blocks, including automatic design configuration, testing and evaluation.
3. Demonstrate knowledge of synthesis options and generate and evaluate synthesis results.
4. Design, simulate, and implement combinational, sequential, and pipelined logic circuit using modern computer-aided design software and programmable logic devices.
5. Consider, compare, and evaluate code segments written using VHDL 2008 vs. VHDL 1993 language elements and verify the CAD tool support.

Topics covered:

1. Functional and Timing ModelSim Simulation using TCL/TK scripts
2. IP Catalog and Components
3. Constraining a designs for speed, area and power optimizations
4. Combinatorial, sequential and pipelined circuits
5. PREP FPLD benchmarks
6. Design Project

Class Schedule: One 165 minute lab per week (1 credit hour).

Subject Area: Engineering

Significant Design: Yes

Relationship to Assessed ABET Student Outcomes: 6(a-d) (CpE only)

Last Updated by: R.J. Perry Date: April 30th, 2021