

ERISC processor Figure /models07/ERISC

of LISA operations = Proc. No. + 4, i.e., ERISC1->5 Op. ... ERISC 13-> 17

Instruction-Set	11	10	9	8	7	6	5	4	3	2	1	0	Assembly Syntax
1	IW												
2	instruction												instruction
3	instruction												
4	0	0	0	0	x	x	x	x	x	x	x	x	"NOP"

ERISC1isa.bmp

Instruction-Set	11	10	9	8	7	6	5	4	3	2	1	0	Assembly Syntax
1	pipe.EXE.IN.PIW												
2	instruction												instruction
3	instruction												
4	0	0	0	0	x	x	x	x	x	x	x	x	"NOP"
5	1	0	1	0	x	x	x	x	x	x	x	x	"SCAN"
6	1	0	1	1	x	x	x	x	x	x	x	x	"PRINT"

ERISC03isa.bmp

#2

Instruction-Set	11	10	9	8	7	6	5	4	3	2	1	0	Assembly Syntax
1	pipe.EXE.IN.PIW												
2	instruction												instruction
3	instruction												
4	0	0	0	0	x	x	x	x	x	x	x	x	"NOP"
5	0	0	0	1	x	x	x	x	x	x	x	x	"ADD"
6	0	0	1	0	x	x	x	x	x	x	x	x	"NEG"
7	0	0	1	1	x	x	x	x	x	x	x	x	"SUB"
8	0	1	0	0	x	x	x	x	x	x	x	x	"MUL"
9	1	0	0	0	imm							"PUSHI" imm	
10	1	0	1	0	x	x	x	x	x	x	x	x	"SCAN"
11	1	0	1	1	x	x	x	x	x	x	x	x	"PRINT"

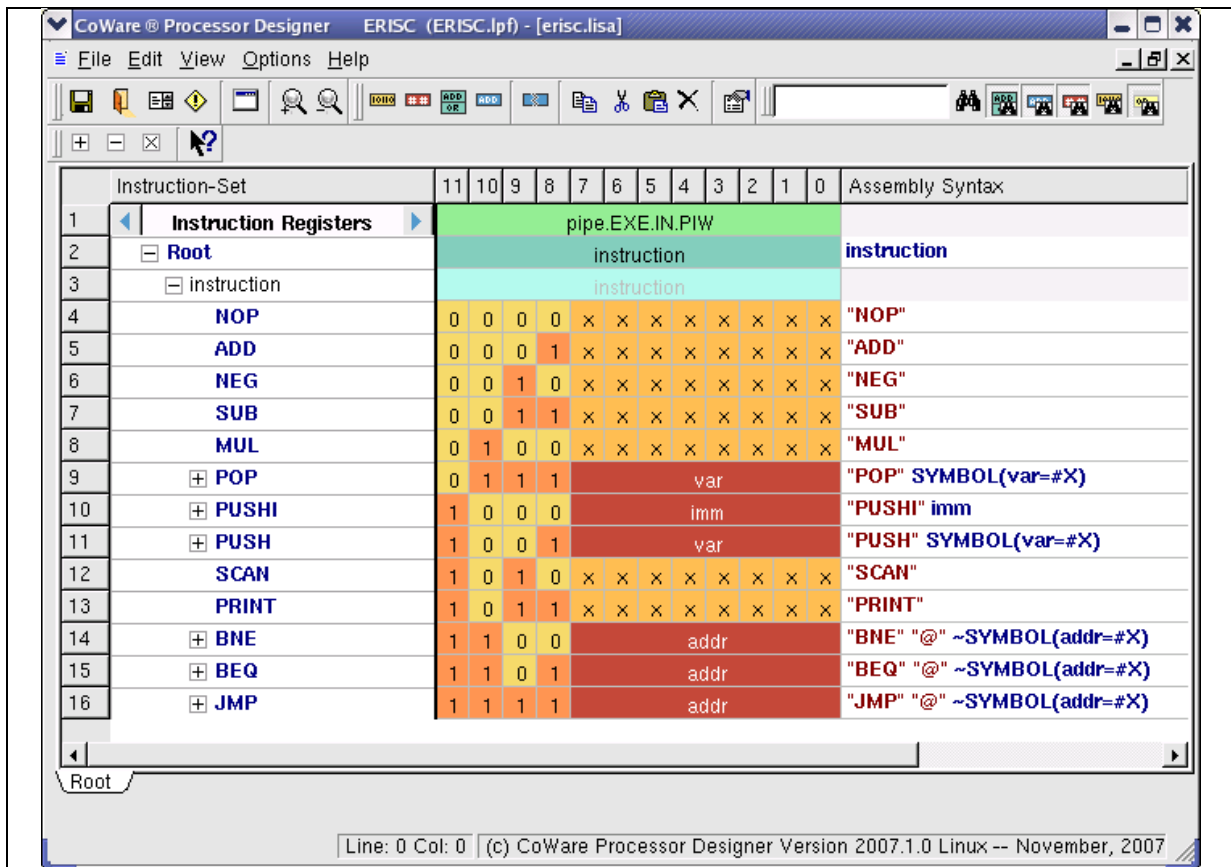
ERISC08isa.bmp

#3

Instruction-Set		11	10	9	8	7	6	5	4	3	2	1	0	Assembly Syntax
1	Instruction Registers	pipe.EXE.IN.PIW												
2	Root	instruction												instruction
3	instruction	instruction												
4	NOP	0	0	0	0	x	x	x	x	x	x	x	x	"NOP"
5	ADD	0	0	0	1	x	x	x	x	x	x	x	x	"ADD"
6	NEG	0	0	1	0	x	x	x	x	x	x	x	x	"NEG"
7	SUB	0	0	1	1	x	x	x	x	x	x	x	x	"SUB"
8	MUL	0	1	0	0	x	x	x	x	x	x	x	x	"MUL"
9	PUSHI	1	0	0	0	imm						"PUSHI" imm		
10	SCAN	1	0	1	0	x	x	x	x	x	x	x	x	"SCAN"
11	PRINT	1	0	1	1	x	x	x	x	x	x	x	x	"PRINT"
12	BNE	1	1	0	0	addr						"BNE" "@" ~SYMBOL(addr=#X)		
13	BEQ	1	1	0	1	addr						"BEQ" "@" ~SYMBOL(addr=#X)		
14	JMP	1	1	1	1	addr						"JMP" "@" ~SYMBOL(addr=#X)		

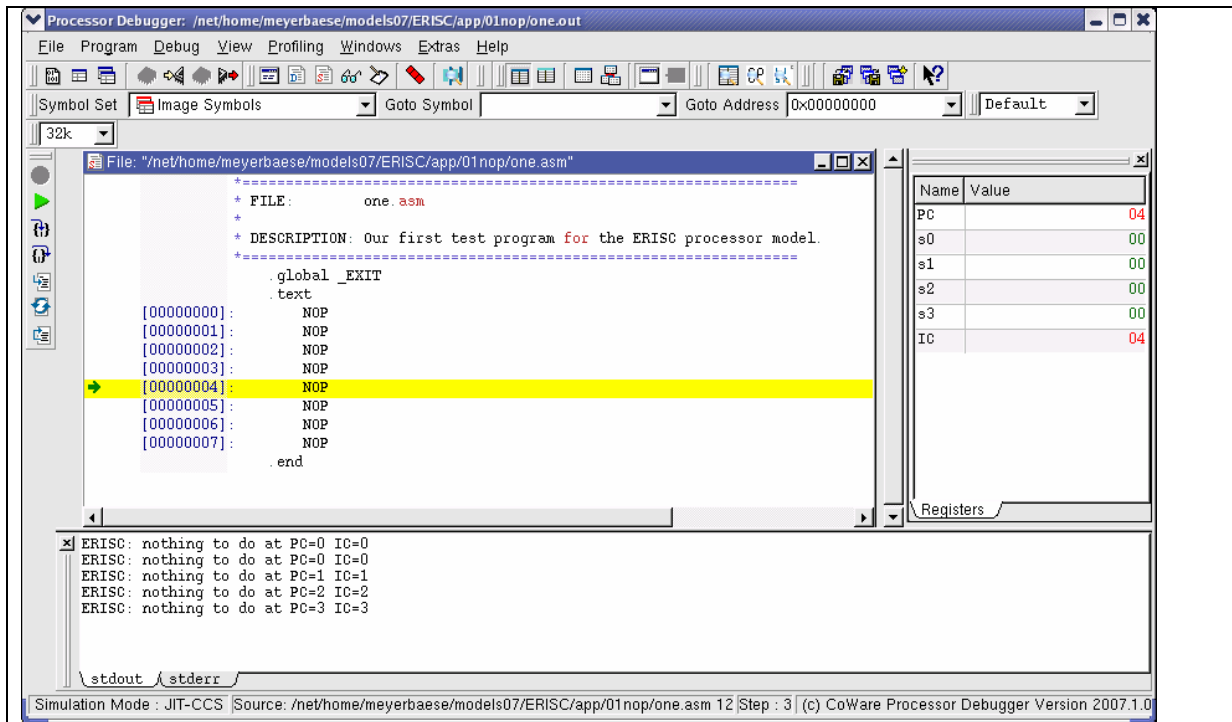
ERISC11isa.bmp

#4



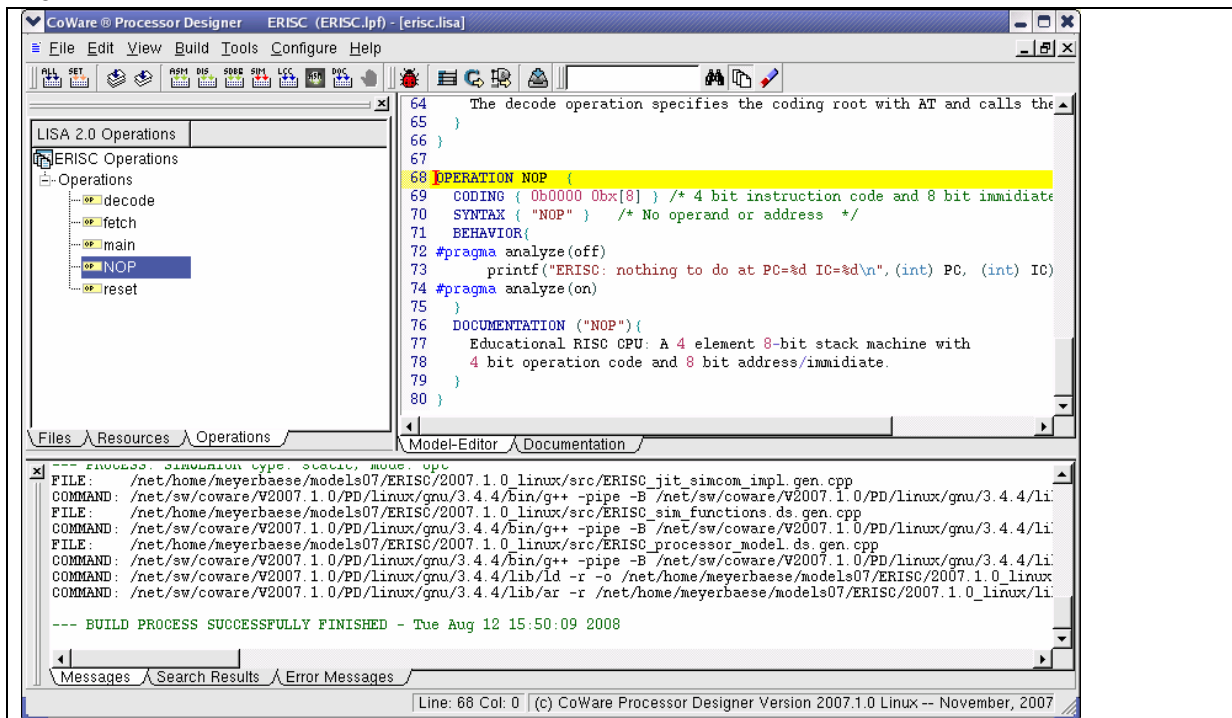
ERISC13isa.bmp

#5



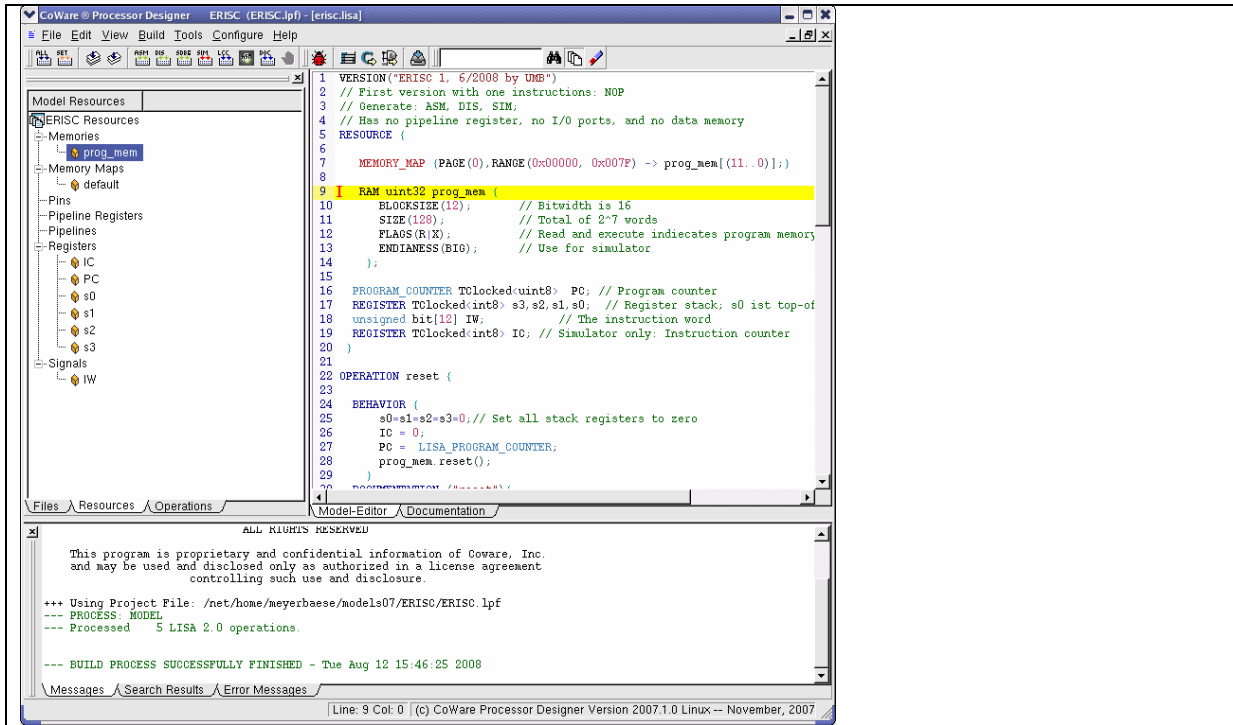
ERISC01debug.bmp

#6



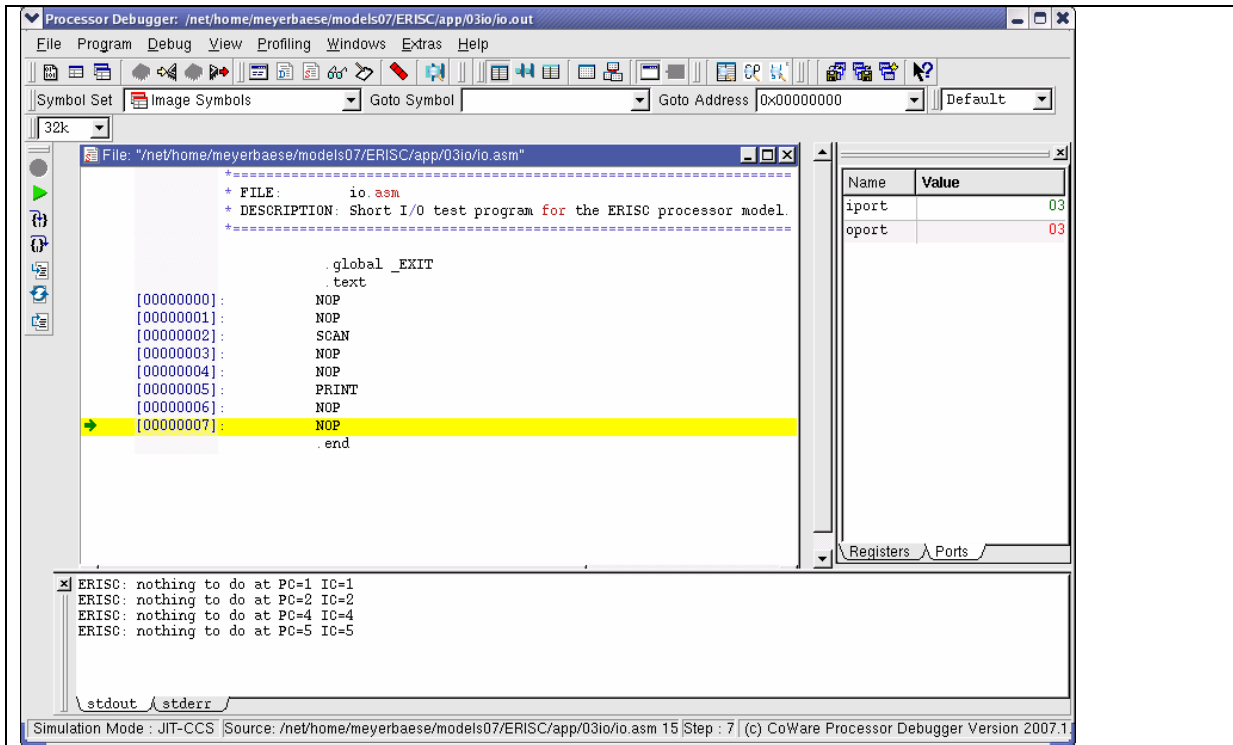
ERISC01codeNOP.bmp

#7



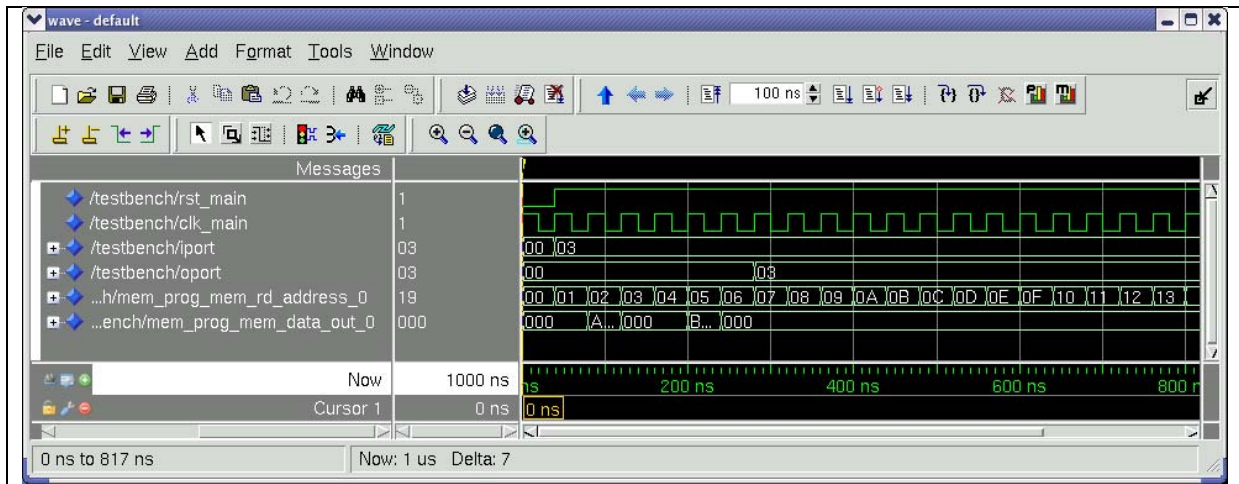
ERISC01code.bmp

#8

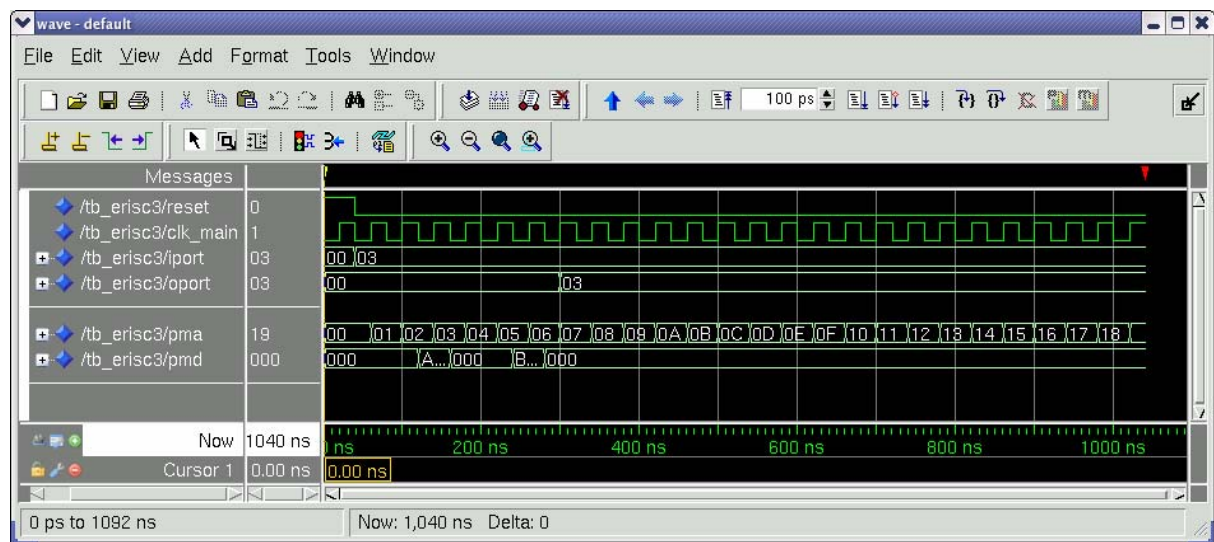


ERISC03debug.bmp

#9

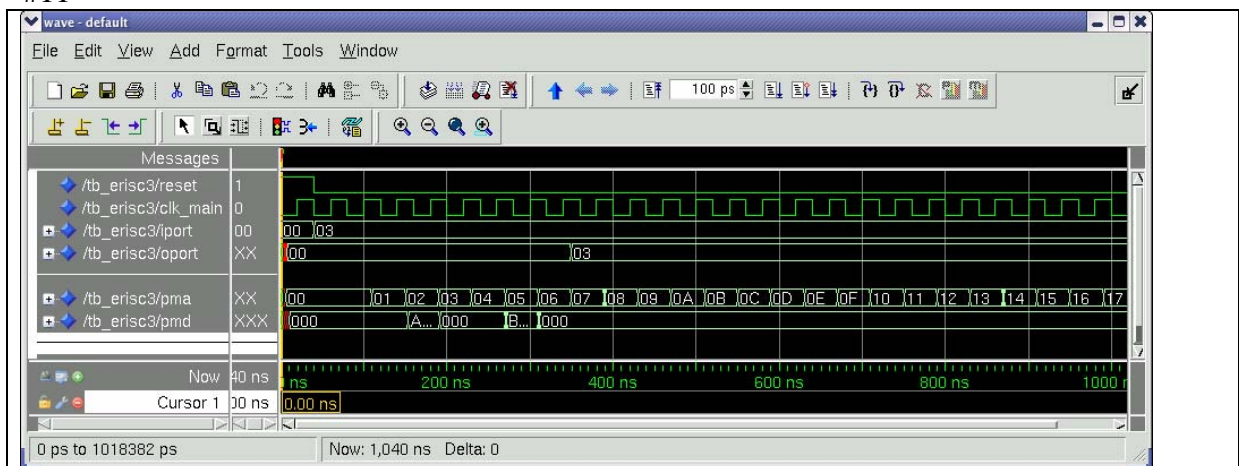


ERISC03funSim.bmp



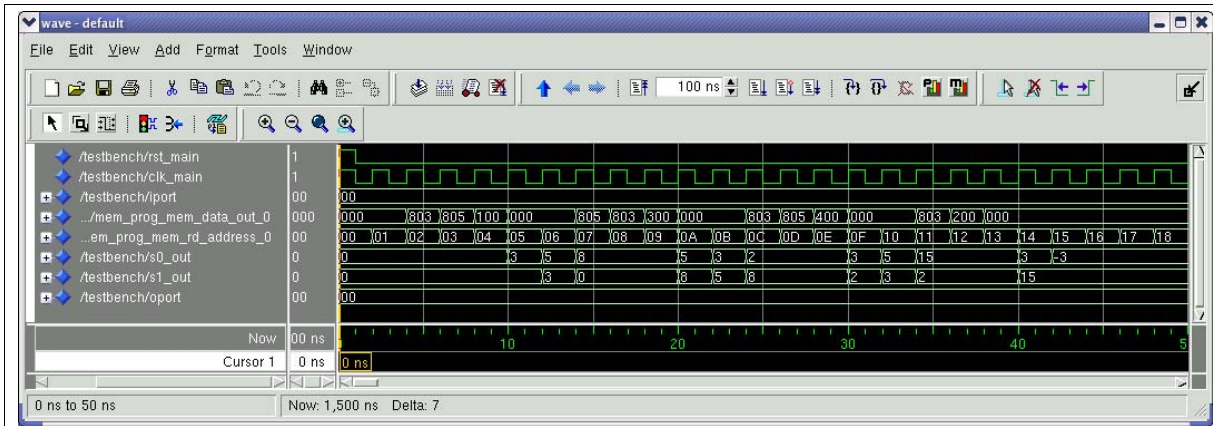
ERISC03xfunSim.bmp

#11



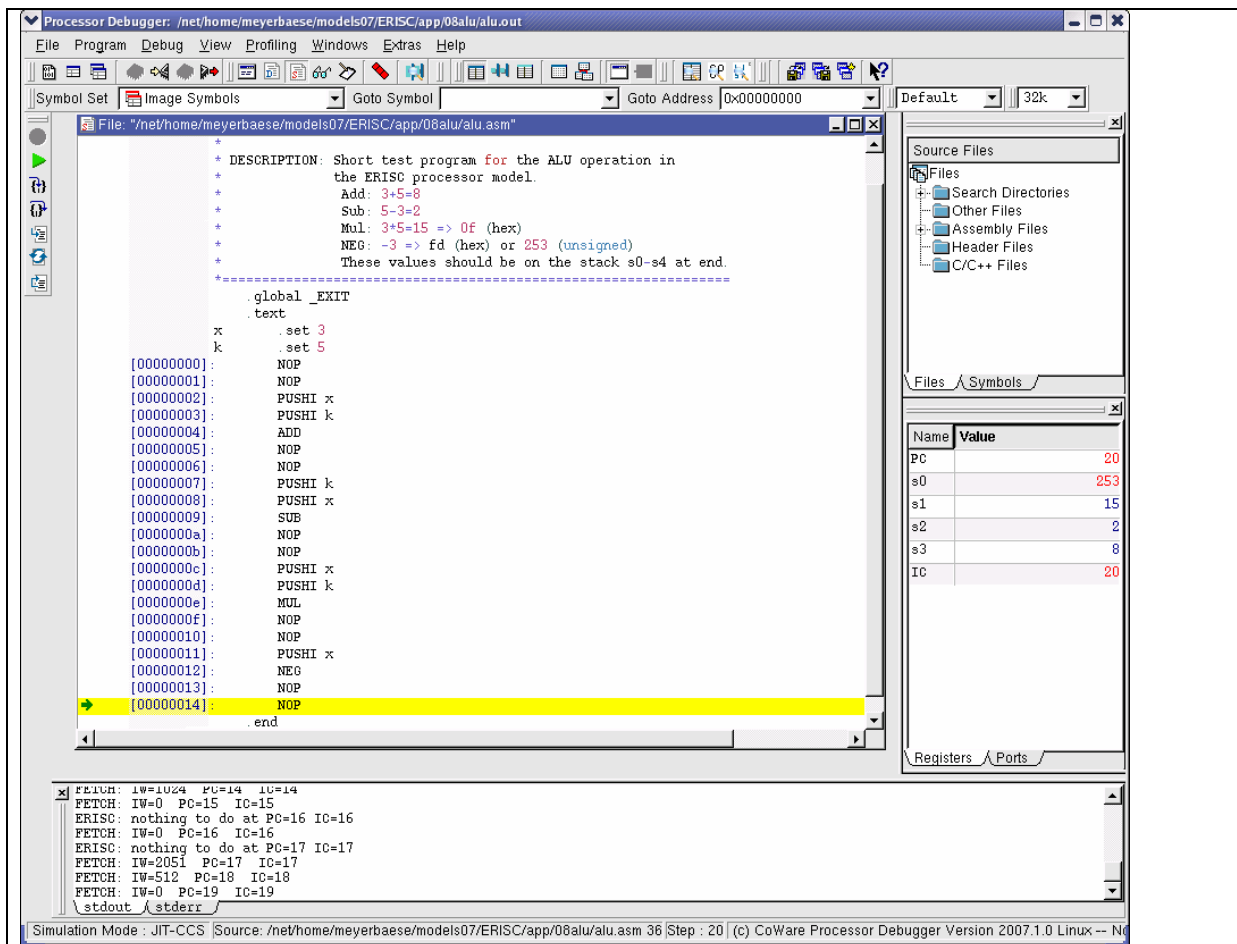
ERISC03xTimingSim.bmp

#12



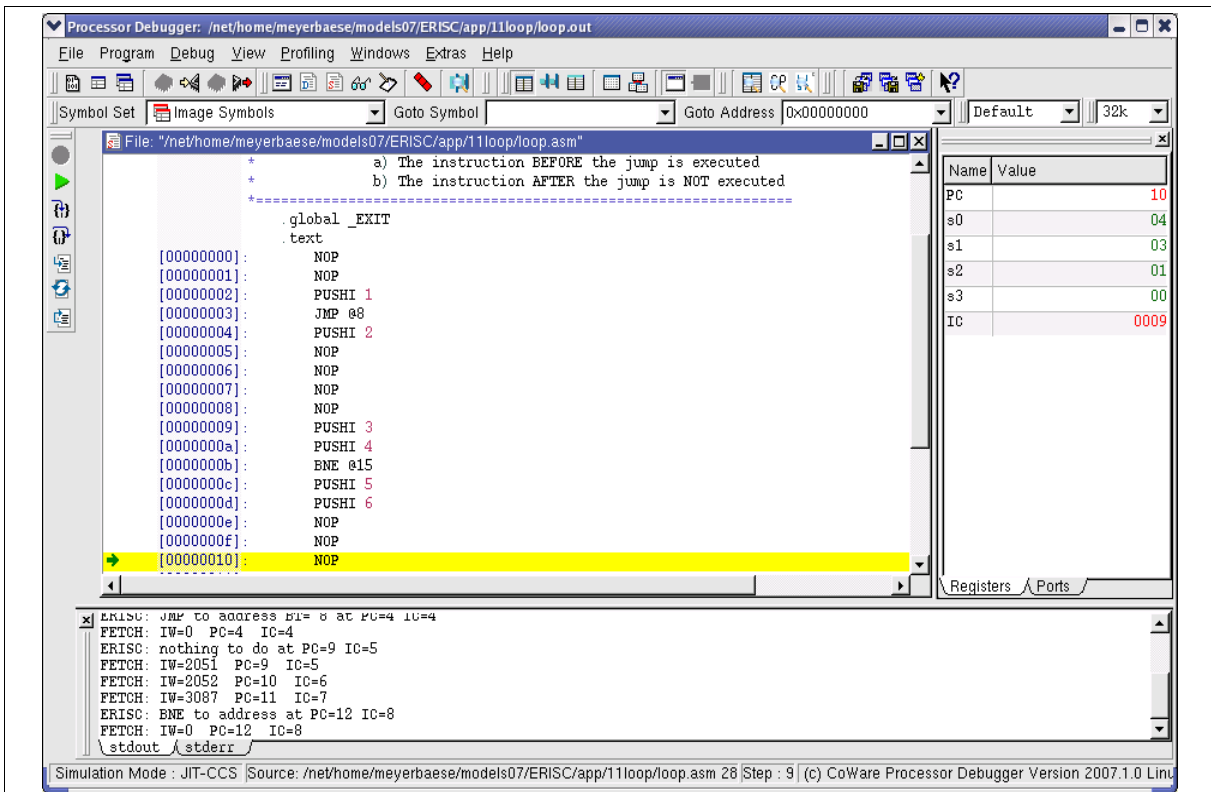
ERISC08funSim.bmp

#13



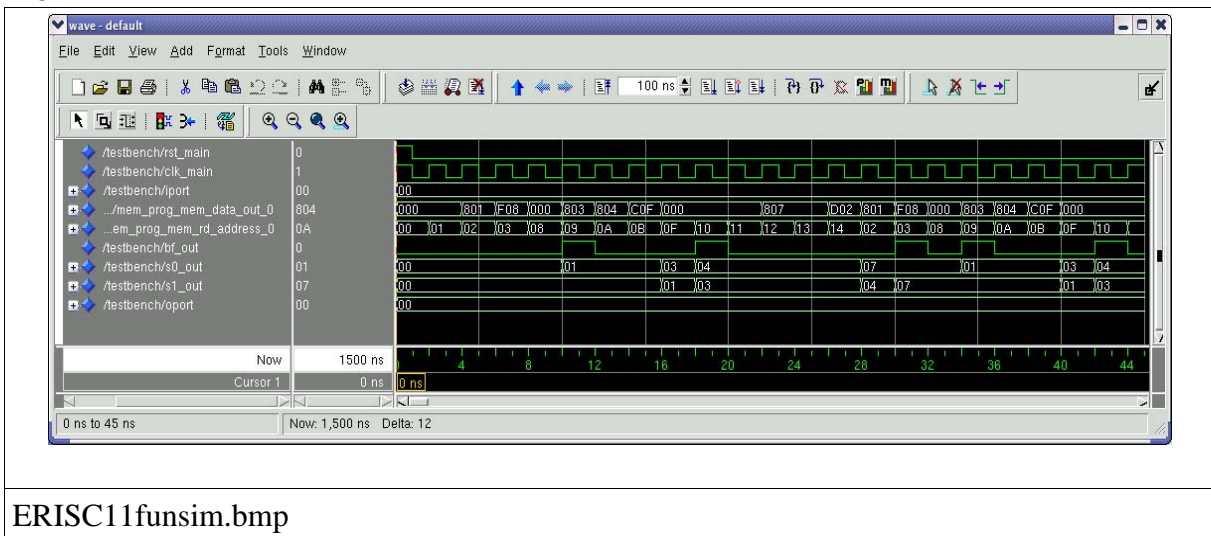
ERISC08debug.bmp

#14



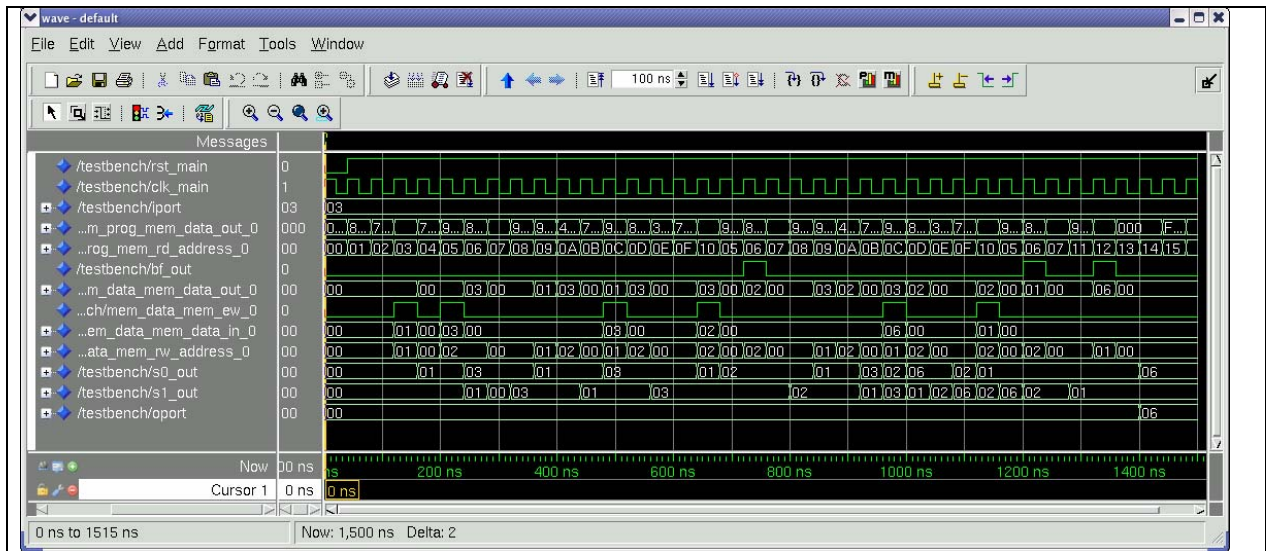
ERISC11debug.bmp

#15



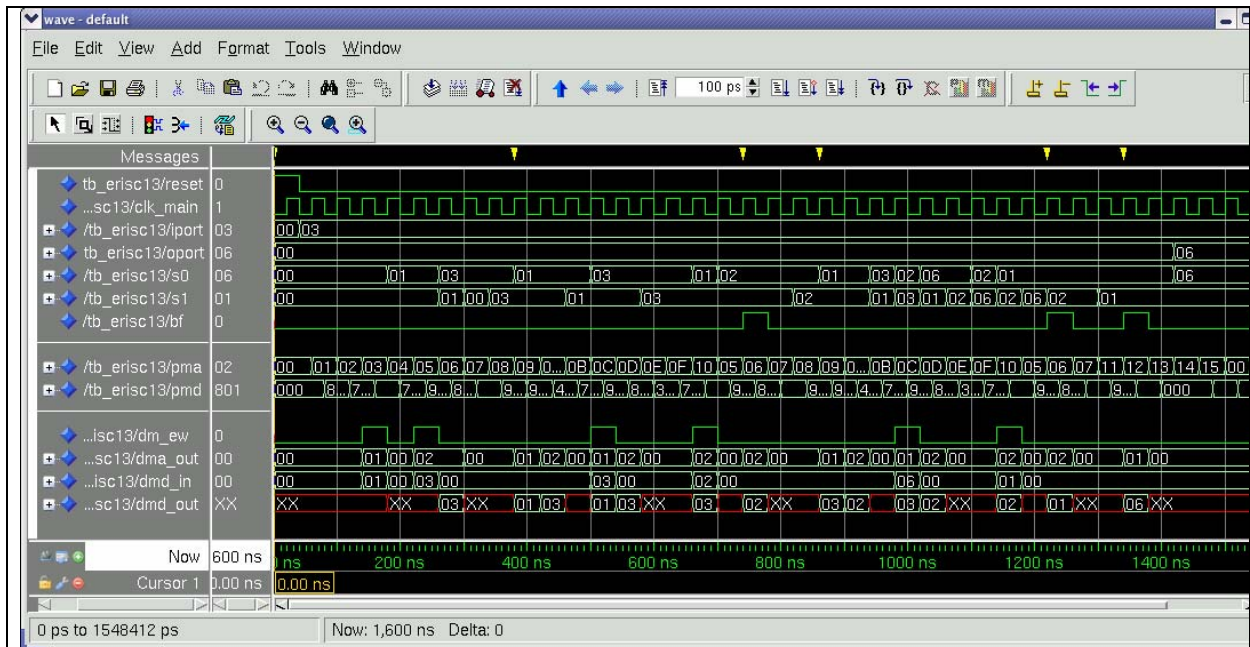
ERISC11funsim.bmp

#16



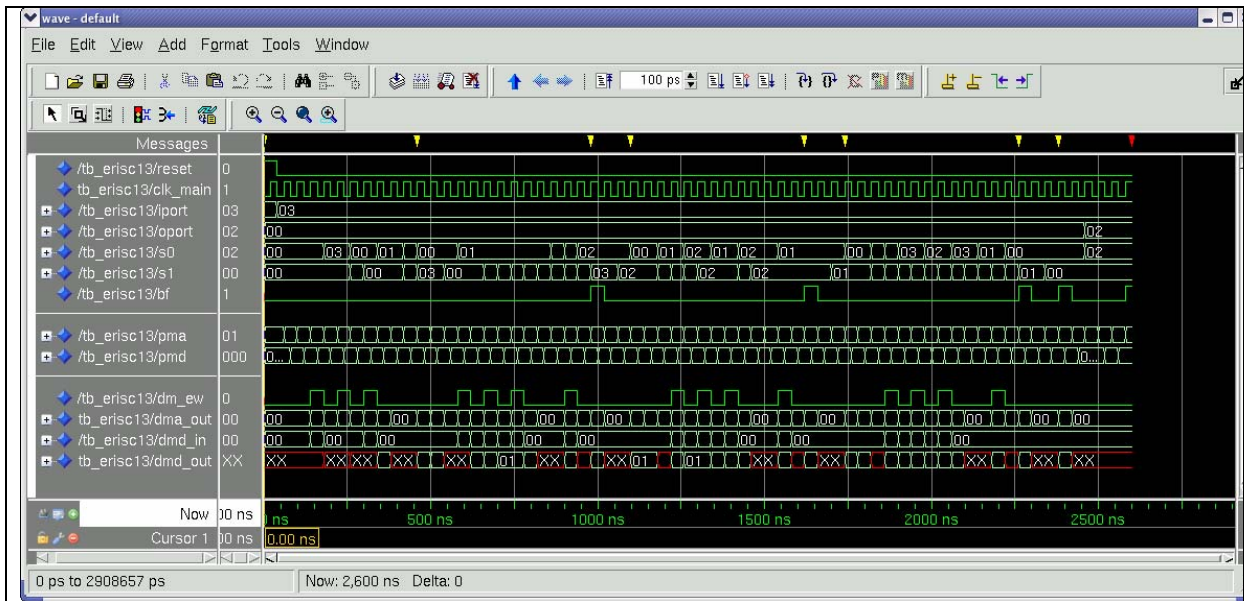
ERISC13funSimFact.bmp

#17



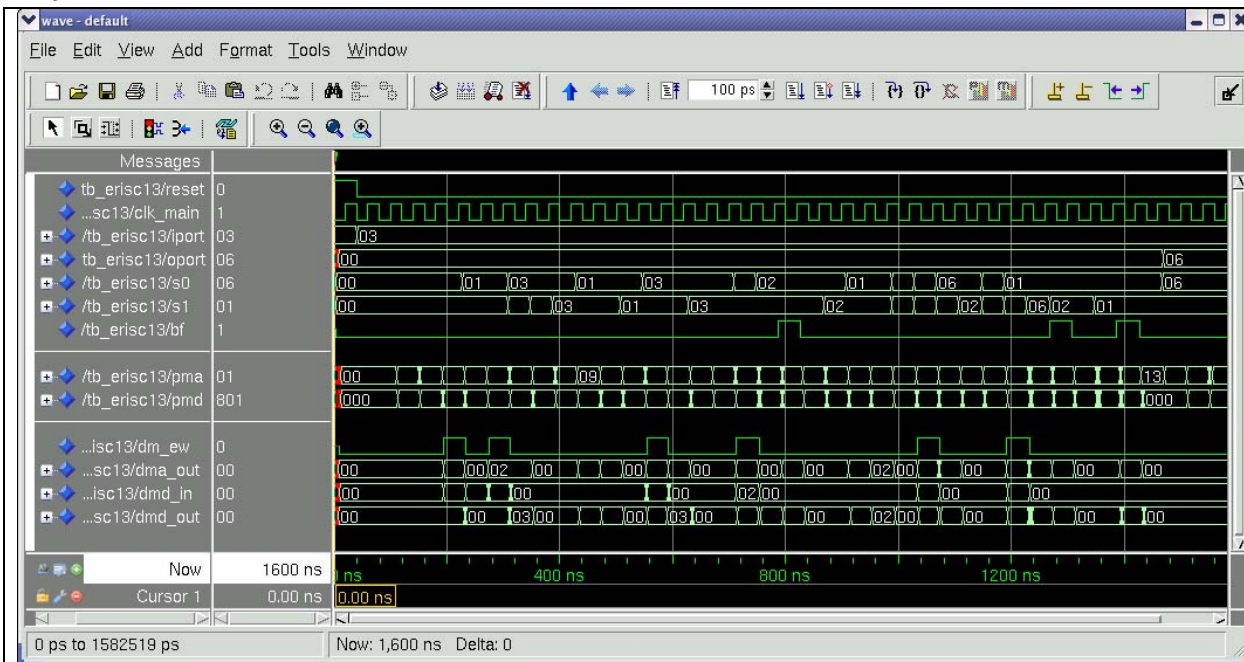
ERISC13xfunSimFact.bmp

#18



ERISC13xfunSimFibo.bmp

#19



ERISC13xTimingSimFact.bmp

#20

Processor Debugger: /net/home/meyerbaese/models07/ERISC/app/13dmtest/dmtest.out

File Program Debug View Profiling Windows Extras Help

Symbol Set Image Symbols Goto Symbol Goto Address 0x00000000

Default 32k

File: "/net/home/meyerbaese/models07/ERISC/app/13dmtest/dmtest.asm"

```

* FILE:      dmtest.asm
* DESCRIPTION: Data memory read (push) and write (pop)
              test program for the ERISC processor model.
*-----*
.global _EXIT
.text
x      .set 1
k      .set 2
[00000000]: NOP
[00000001]: NOP
[00000002]: PUSHI 5
[00000003]: NOP
[00000004]: POP k
[00000005]: NOP
[00000006]: PUSHI 1
[00000007]: NOP
[00000008]: NOP
[00000009]: PUSH k
[0000000a]: NOP
[0000000b]: NOP

```

Source Files

- Files
 - Search Director...
 - Other Files
 - Assembly Files
 - Header Files
 - C/C++ Files

Files Symbols

Name	Value
PC	0b
s0	05
s1	01
s2	05
s3	00
IC	0b

Registers Ports

Memories

A	C	B	E	I	Display	Address												
Address	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	ASCII	
00000000	00	00	05	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
00000010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	

data mem prog mem

```

ERISC: nothing to do at PC=6 IC=6
FETCH: IW=2049 PC=6 IC=6
ERISC: nothing to do at PC=7 IC=7
FETCH: IW=0 PC=7 IC=7
ERISC: nothing to do at PC=8 IC=8
FETCH: IW=0 PC=8 IC=8
ERISC: nothing to do at PC=8 IC=8
FETCH: IW=0 PC=8 IC=8
ERISC: nothing to do at PC=9 IC=9
FETCH: IW=2306 PC=9 IC=9
ERISC: nothing to do at PC=9 IC=9
FETCH: IW=0 PC=9 IC=9
ERISC: nothing to do at PC=10 IC=10
FETCH: IW=0 PC=10 IC=10

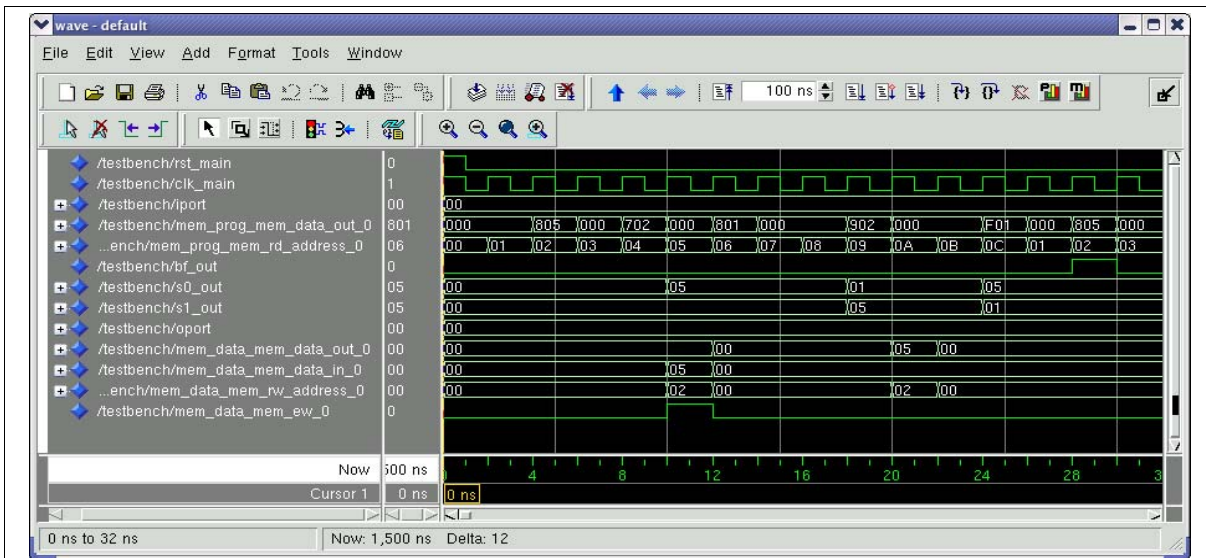
```

stdout stderr

Simulation Mode: JIT-CCS Source: /net/home/meyerbaese/models07/ERISC/app/13dmtest/dmtest.asm 22 Step: 11 (c) CoWare Proc

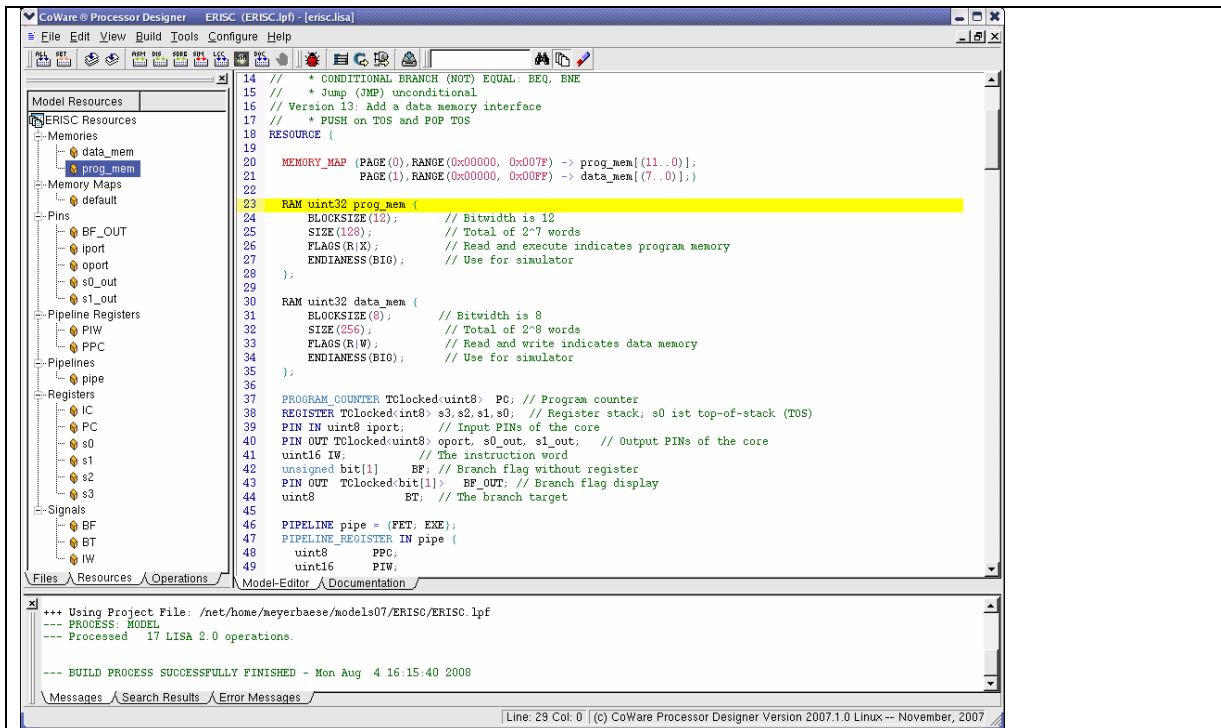
ERISC13debugDMtest.bmp

#23



ERISC13funSimDMtest.bmp

#24



ERISC13code.bmp

#25

August 2008

