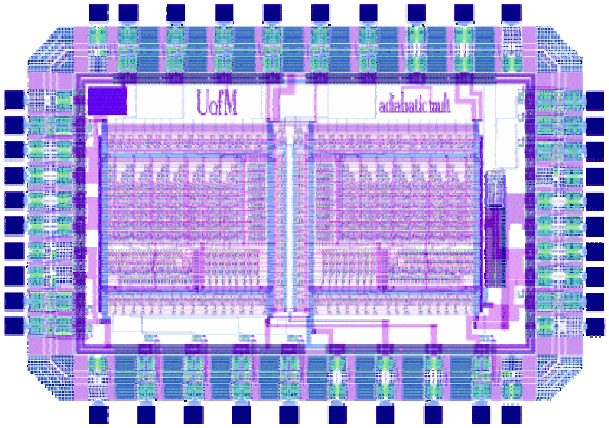
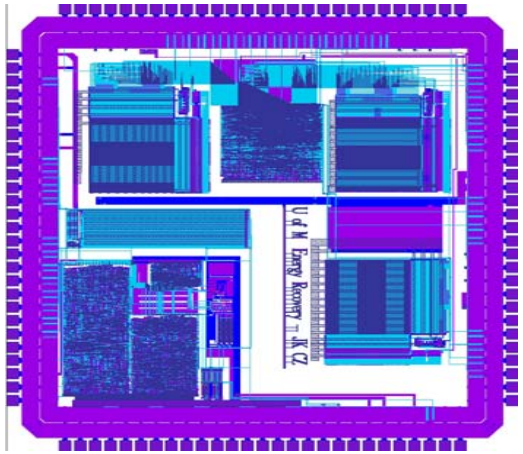
Fast, Efficient, Recovering, and Irreversible





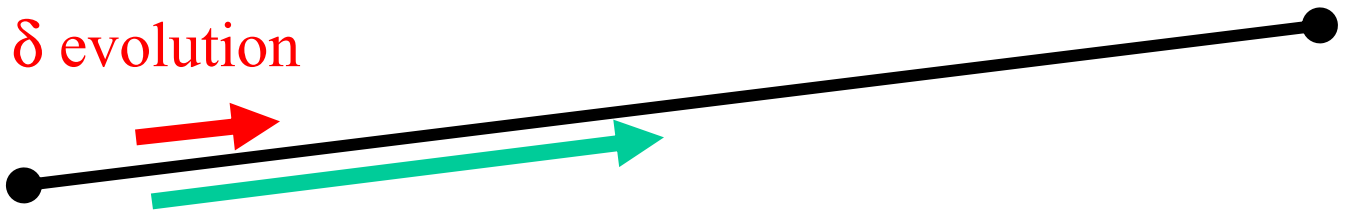
V. Sathe, J.-Y. Chueh, J. Kim, C. Ziesler*, S. Kim**,
Marios Papaefthymiou

Advanced Computer Architecture Laboratory
EECS Department
University of Michigan

Currently at *MultiGig, Inc and **Seoul National University

On the Path to Logic Reversibility

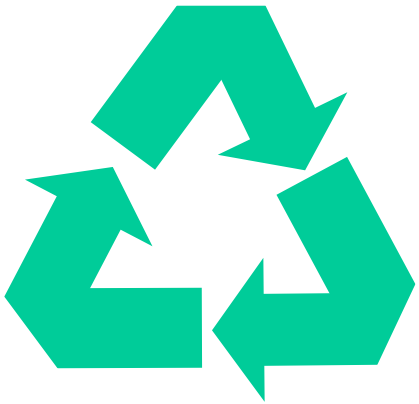
Charge recovery CMOS
Reversible logic



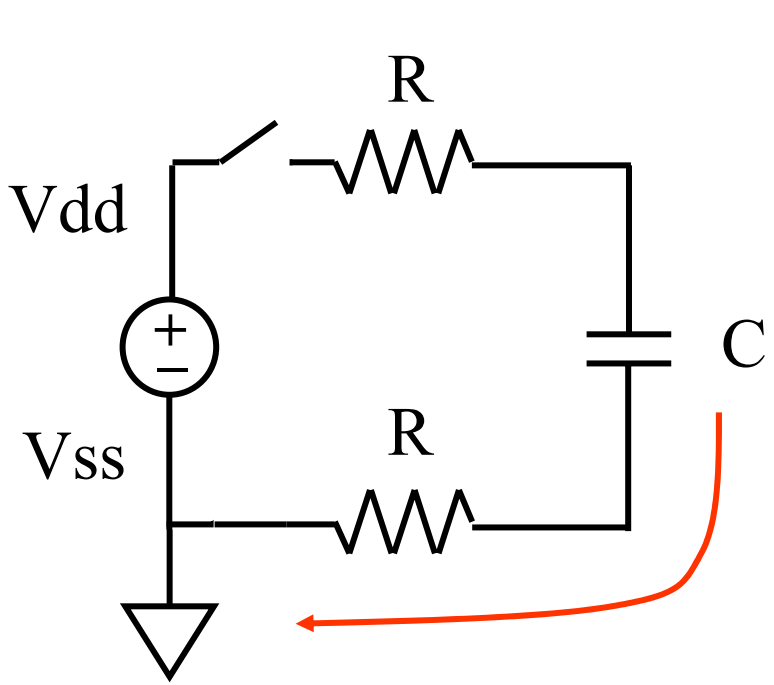
Conventional CMOS
Irreversible logic

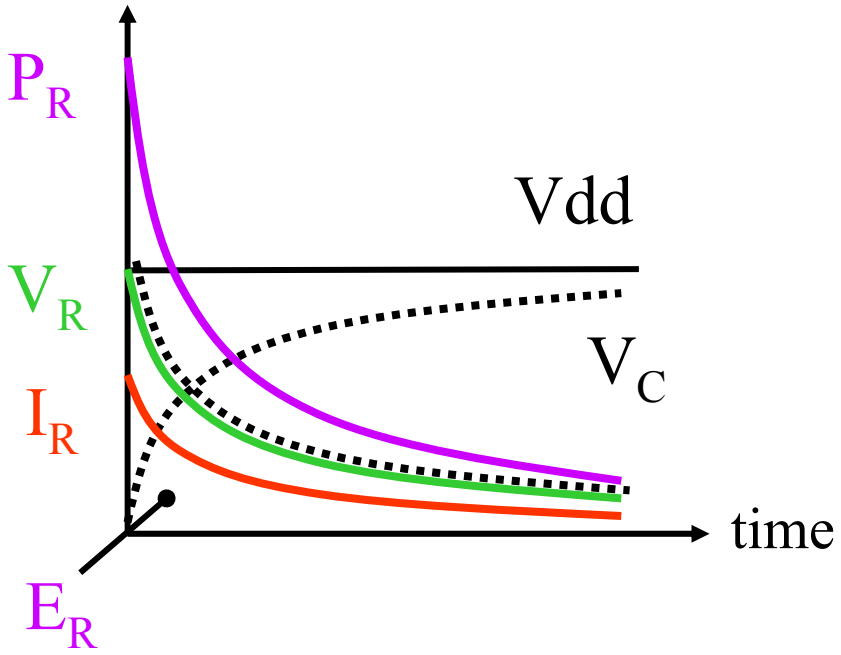
Charge recovery CMOS
Irreversible logic

- "physical" reversibility (energy recycling)
- high speed
- practical implementation



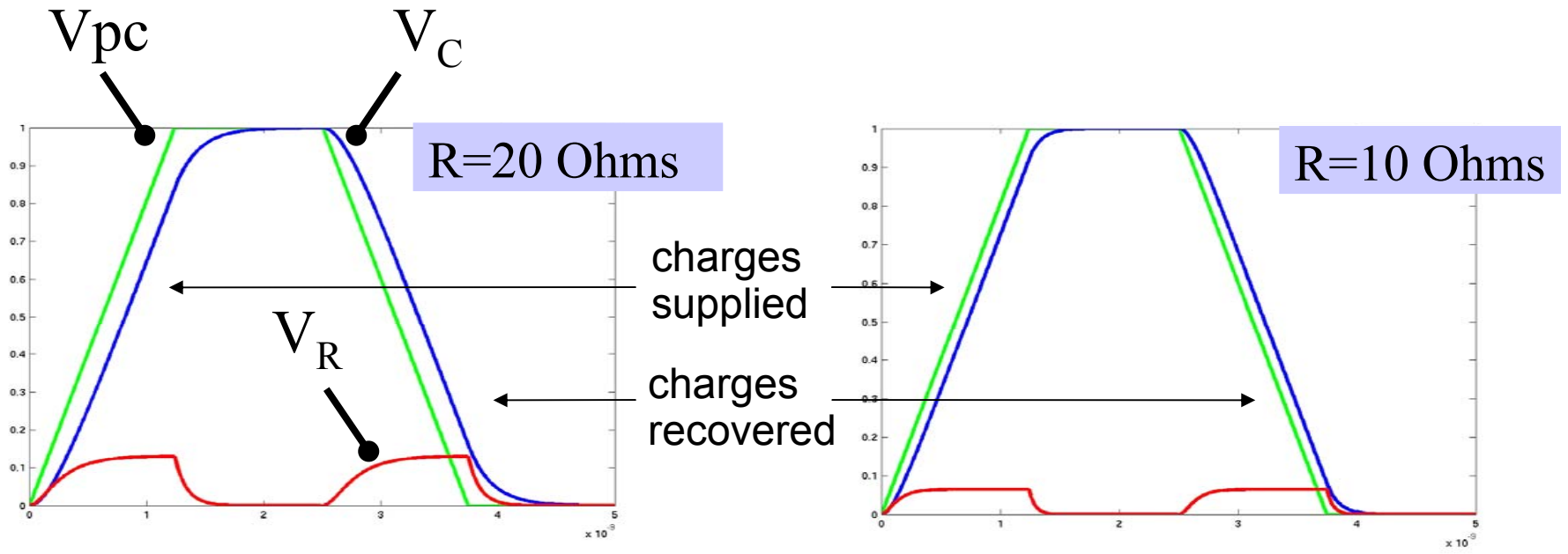
Conventional CMOS Operation



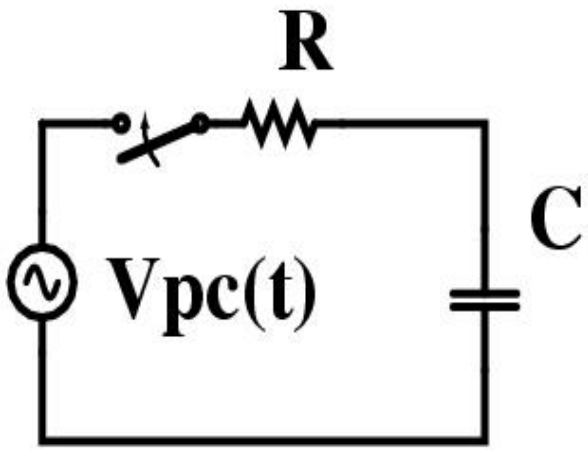


- Constant supply voltage Vdd
- One-way street to ground
- High voltage drops across conducting devices
- Energy dissipation grows with CV^2

Charge Recovery



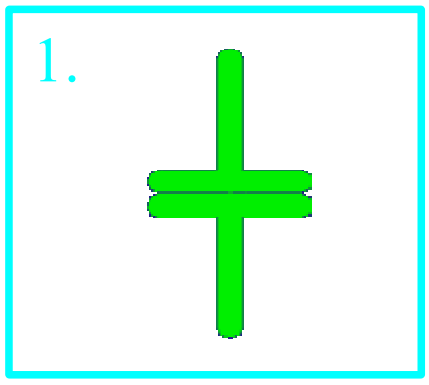
- Time-varying "power-clock" Vpc
- Charge recovered from load C
- Charge transfer through R takes time T
- Power dissipated on R
- Energy dissipation grows with (RC/T) CV^2
- Reducing R decreases dissipation
- Increasing T decreases dissipation

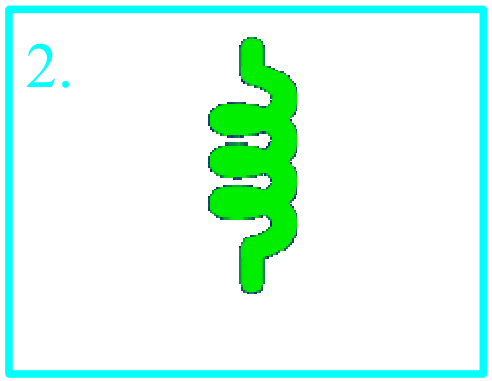


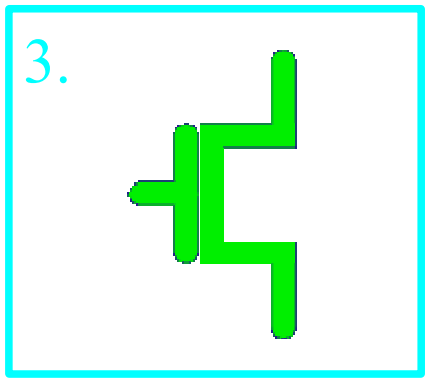
The Design Space

Complex web of intertwined issues

1. Which capacitance to recover from?
   - Clock network? Gates? Bit lines? I/O? Other?
   - Balancing? Other issues?
2. How to store/reuse recovered energy?
   - Capacitors? Inductors?
   - How many power-clock phases?
3. What circuits do the recovery?
   - Power-clock generator design







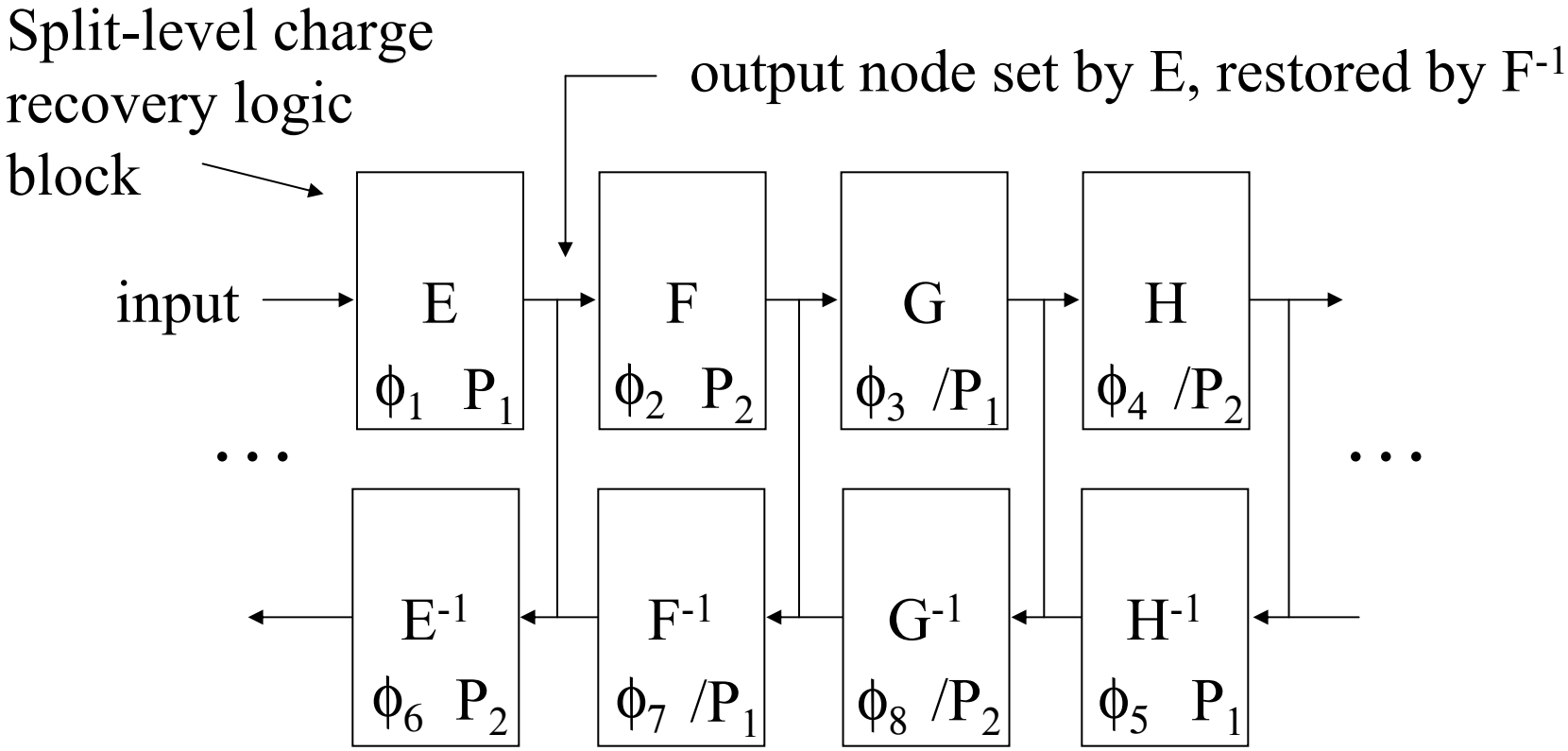
Sample Design Points from'90s

- Asymptotically zero-energy split-level charge recovery logic
  S.G. Younis and T. F. Knight, Jr. – SPLE'94

- Clock-powered CMOS: A hybrid adiabatic logic style for energy-efficient computing
  N. Tzartzanis and W. C. Athas – ARVLSI'99

And many, many others....
Few real working chips, however.

Example: Reversible Pipelines



- Gate outputs are restored using a reverse pipeline whose elements perform the inverse function of the forward pipeline
- Reversibility overheads aside, multiple phases result in high design complexity

The Michigan Designs

- Multiplier chip (2001)

  Semi-custom dynamic circuitry with fine-grain recovery from gate outputs

- Discrete wavelet transform chip (2003)

  Standard-cell ASIC design with recovery of clock power

- GHz-class chip (2005)

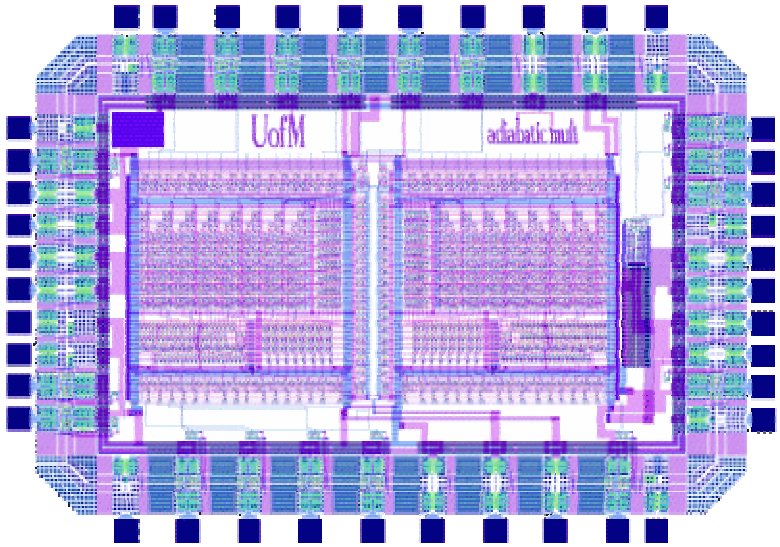
  Semi-custom dynamic circuitry with fine-grain recovery from gate outputs and near-threshold supply voltage scaling

- Guiding principles
  - Simplicity
  - Minimal control and hardware overhead

- Key attributes
  - Sinusoidal power-clock for power and synchronization
  - Integrated power-clock generator
  - High operating speeds (1GHz in silicon)
  - Higher energy efficiency than conventional counterparts

Multiplier Chip

- Suhwan Kim and Conrad Ziesler (while at UM) received First Prize in VLSI Design Contest, DAC 2001.

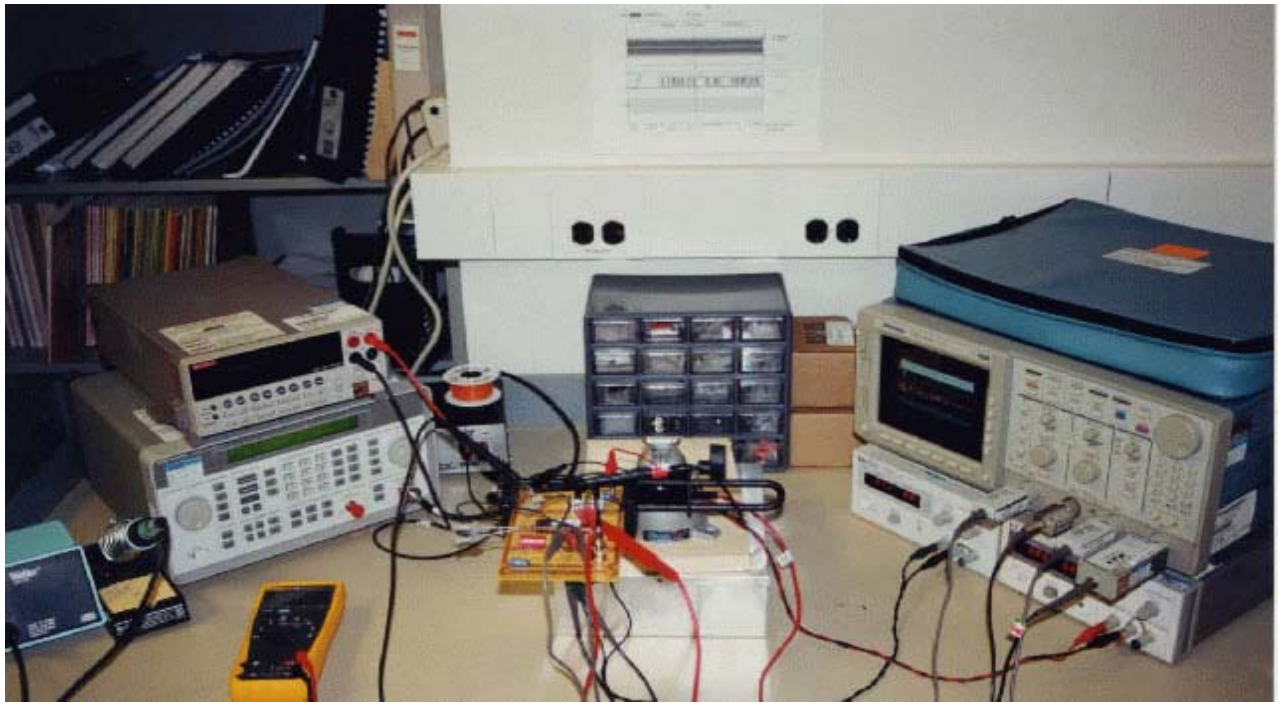


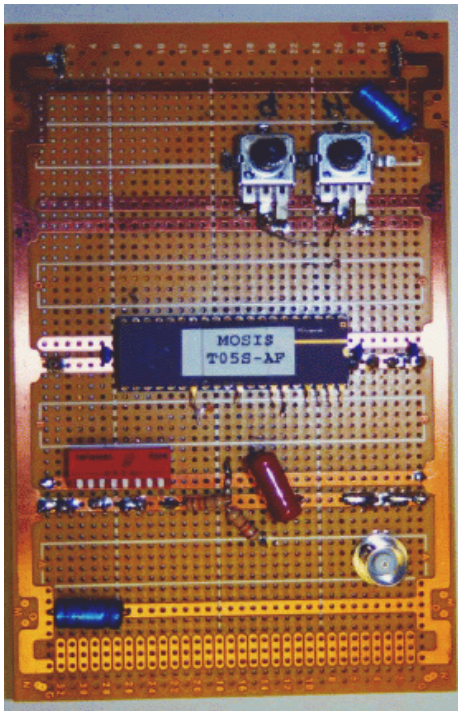
- Minimalist approach
  - Simple tools: magic and spice
  - Low-cost standard CMOS process: HP 0.5µm, 40-pin DIP package, through MOSIS.

- Operational chip demonstrates practicality of energy-recovering circuit design
  - Non-trivial size (8-bit operands, on-chip clock, self-test)
  - High throughput
  - Low energy dissipation

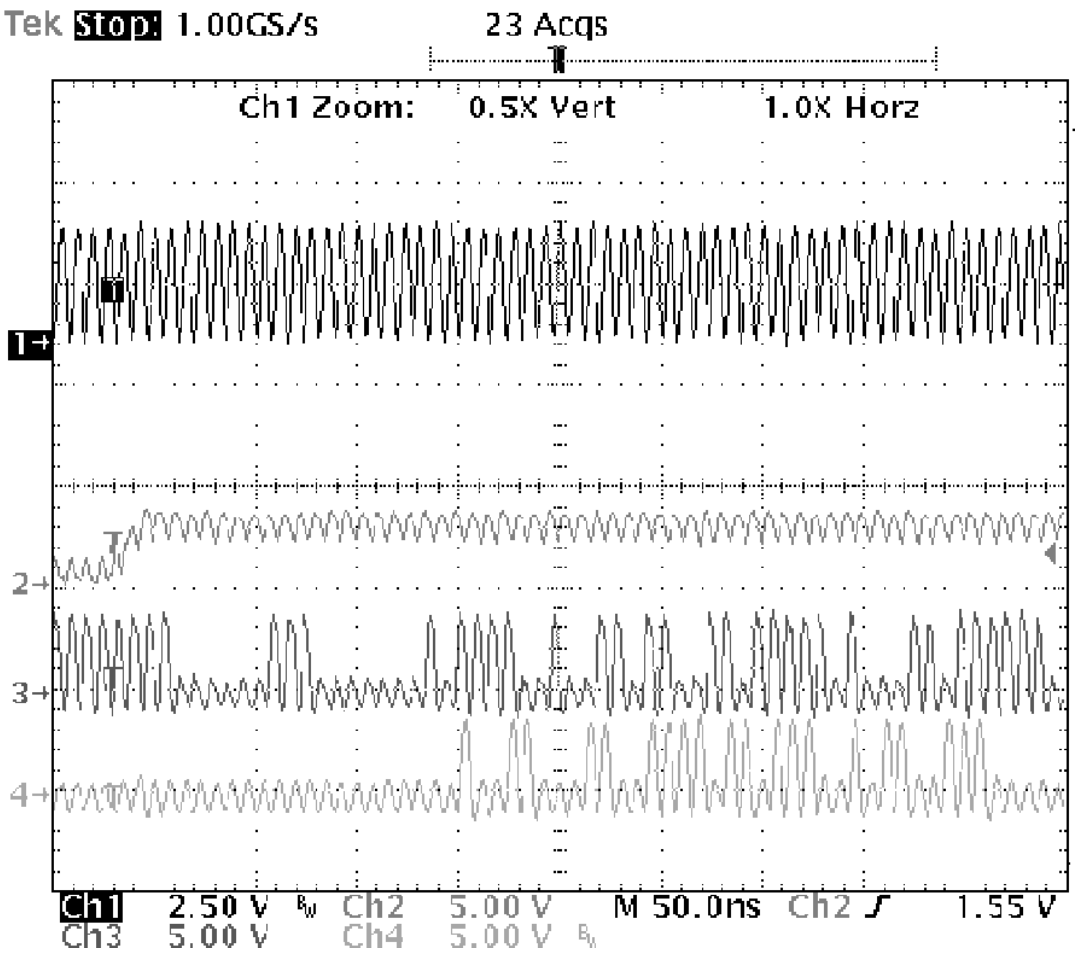
Low-Energy High-Speed Operation

- Working 1st silicon
- Simple yet effective experimental setup.
- Correct operation verified @ 130 MHz.
- Energy efficient operation validated by measurements.





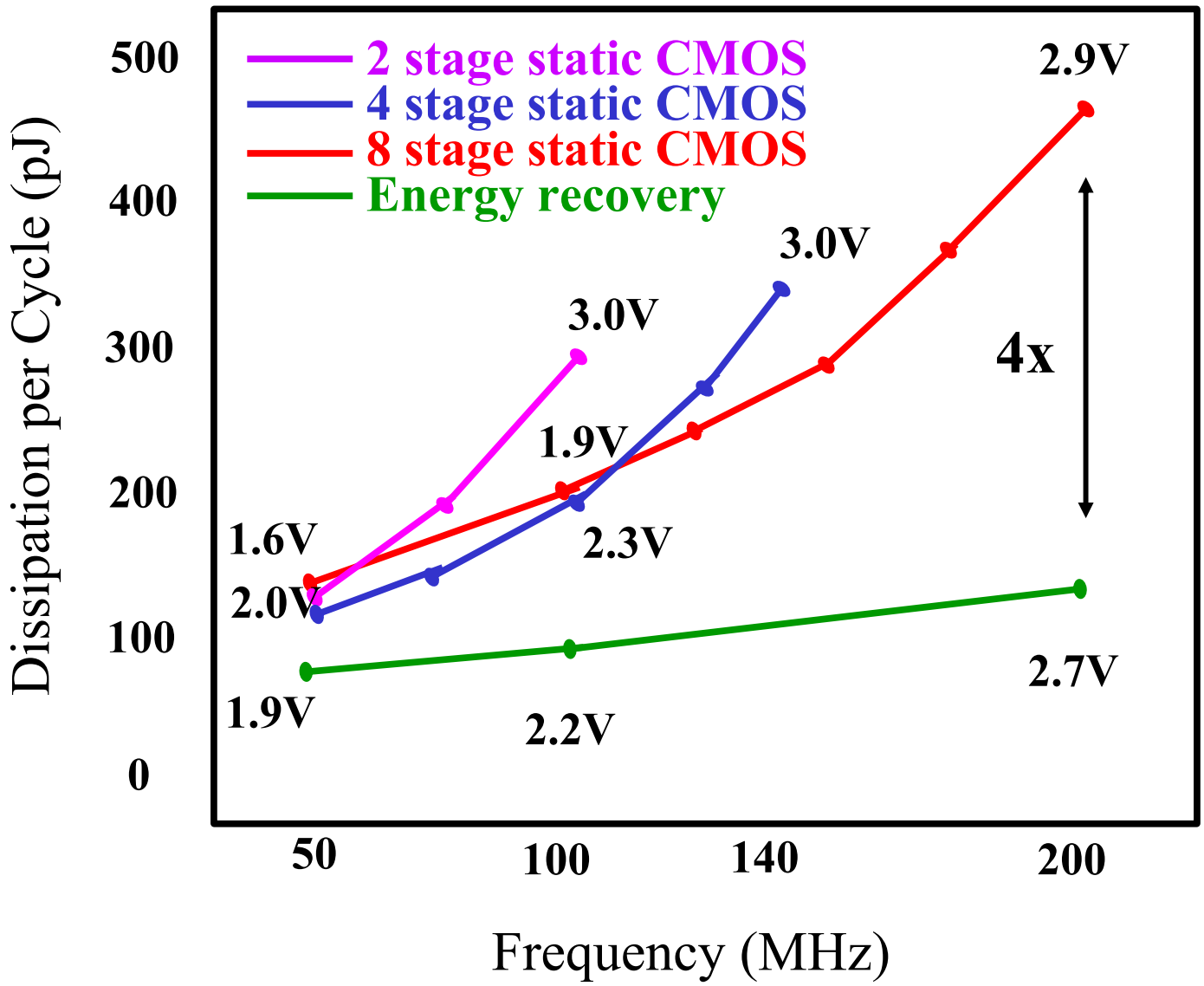
Correct Function



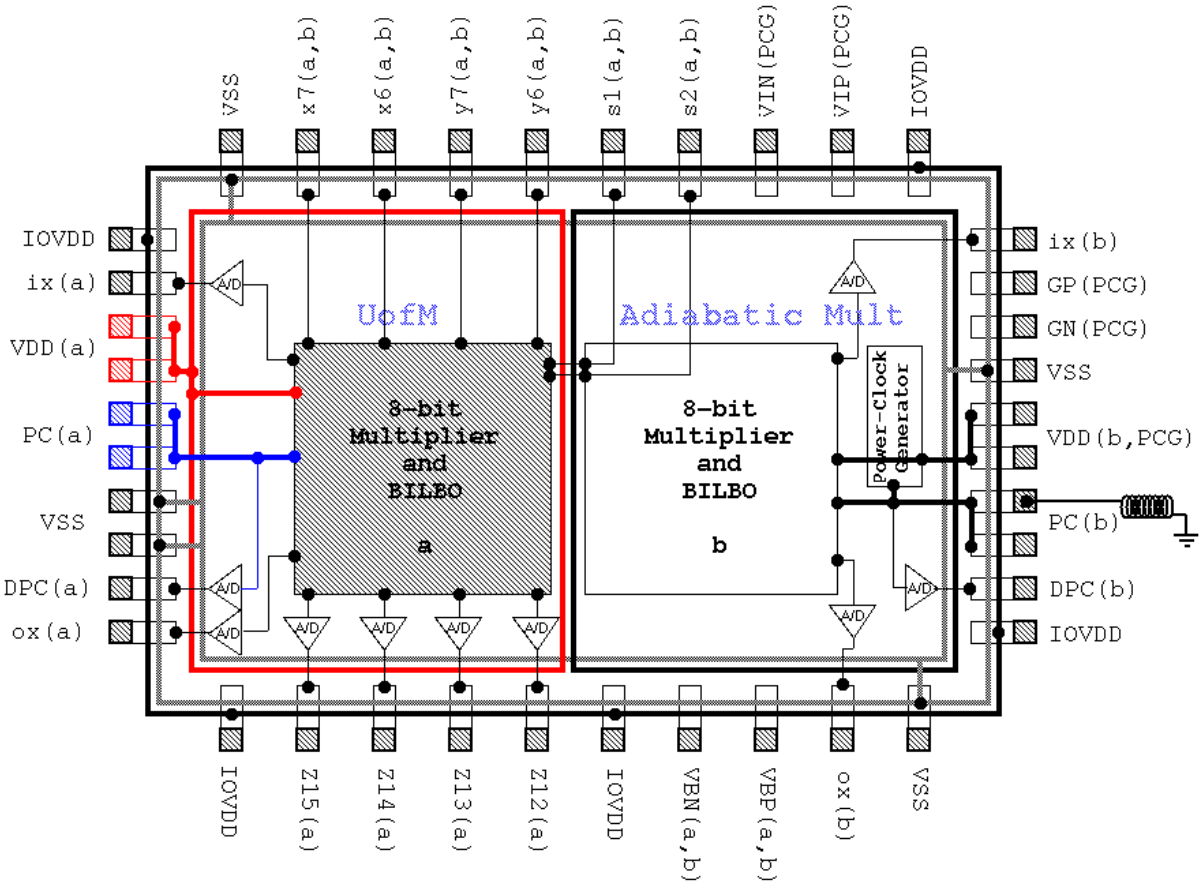
130MHz

signature output

Energy Comparison

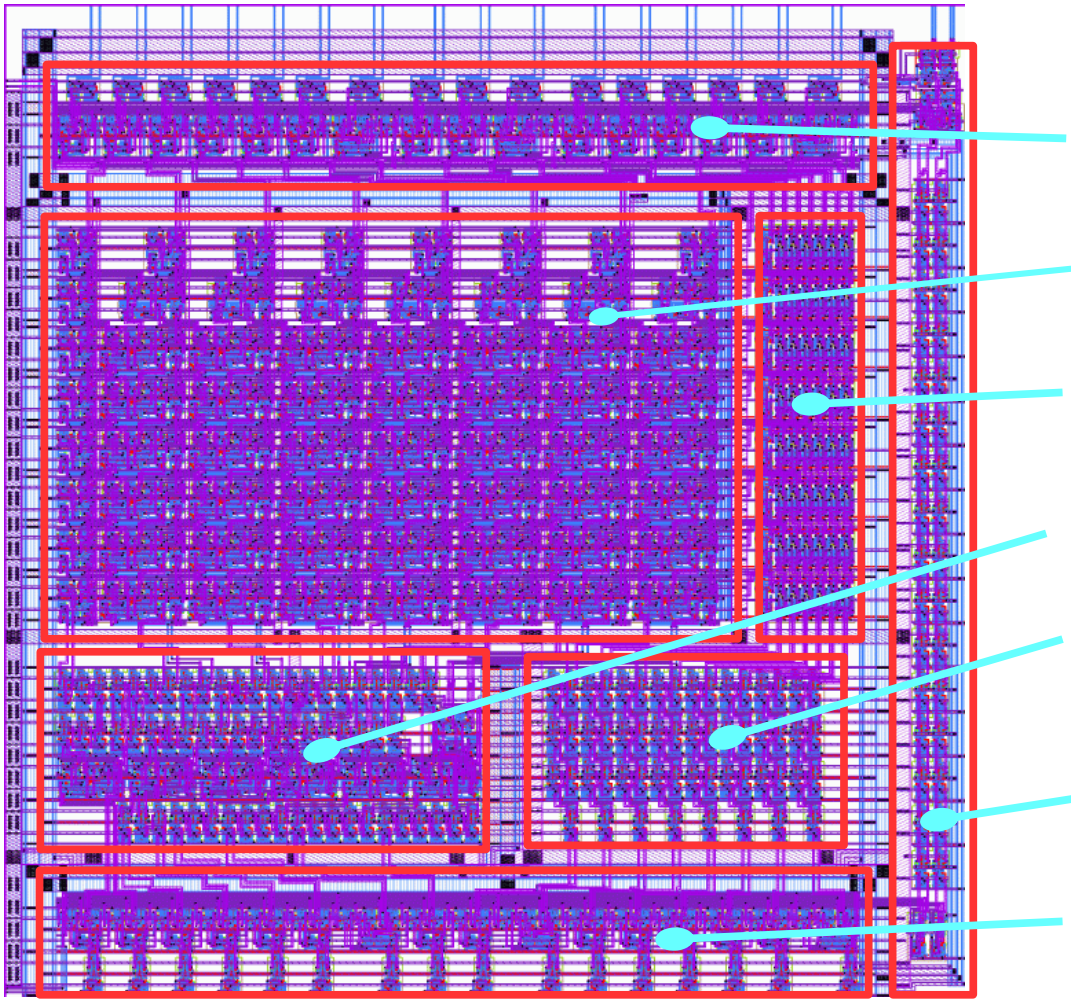


Test Chip Overview



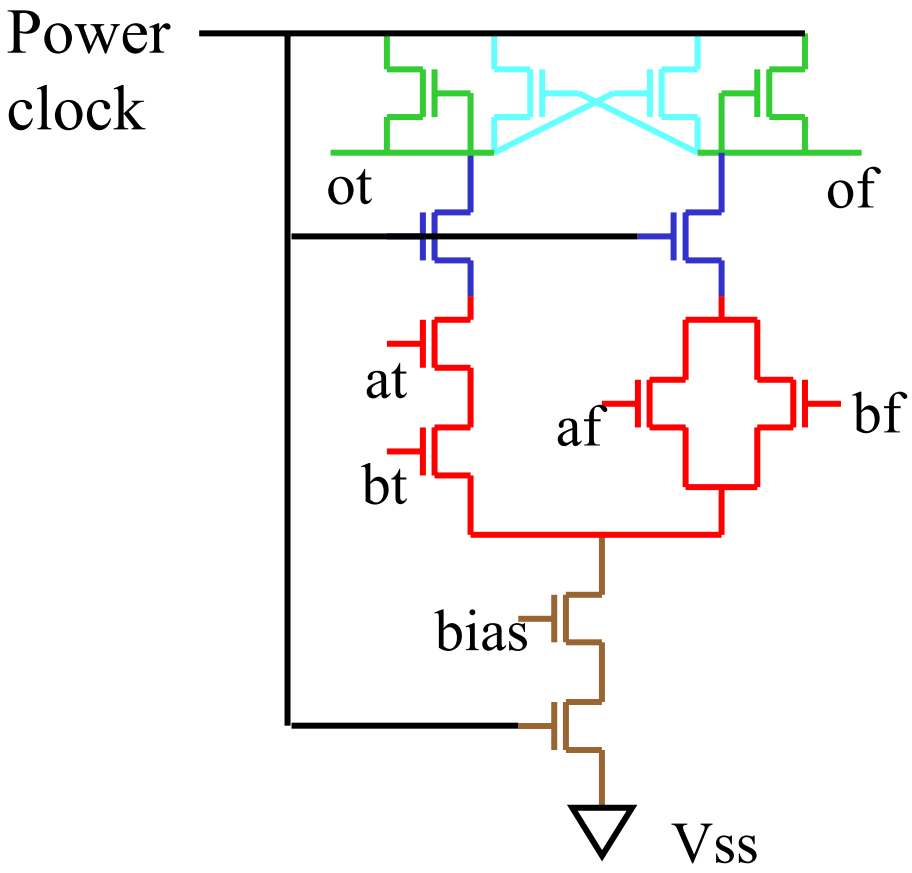
- Two multipliers with self-test per chip (minimum size die)
- Integrated power-clock generator
- Resonant LC oscillator

Multiplier and Self-Test



- 9,048 devices in multiplier array, 2,806 devices in self-test circuitry
- Implemented entirely in energy-recovering dynamic logic family.

Energy-Recovering Dynamic Logic

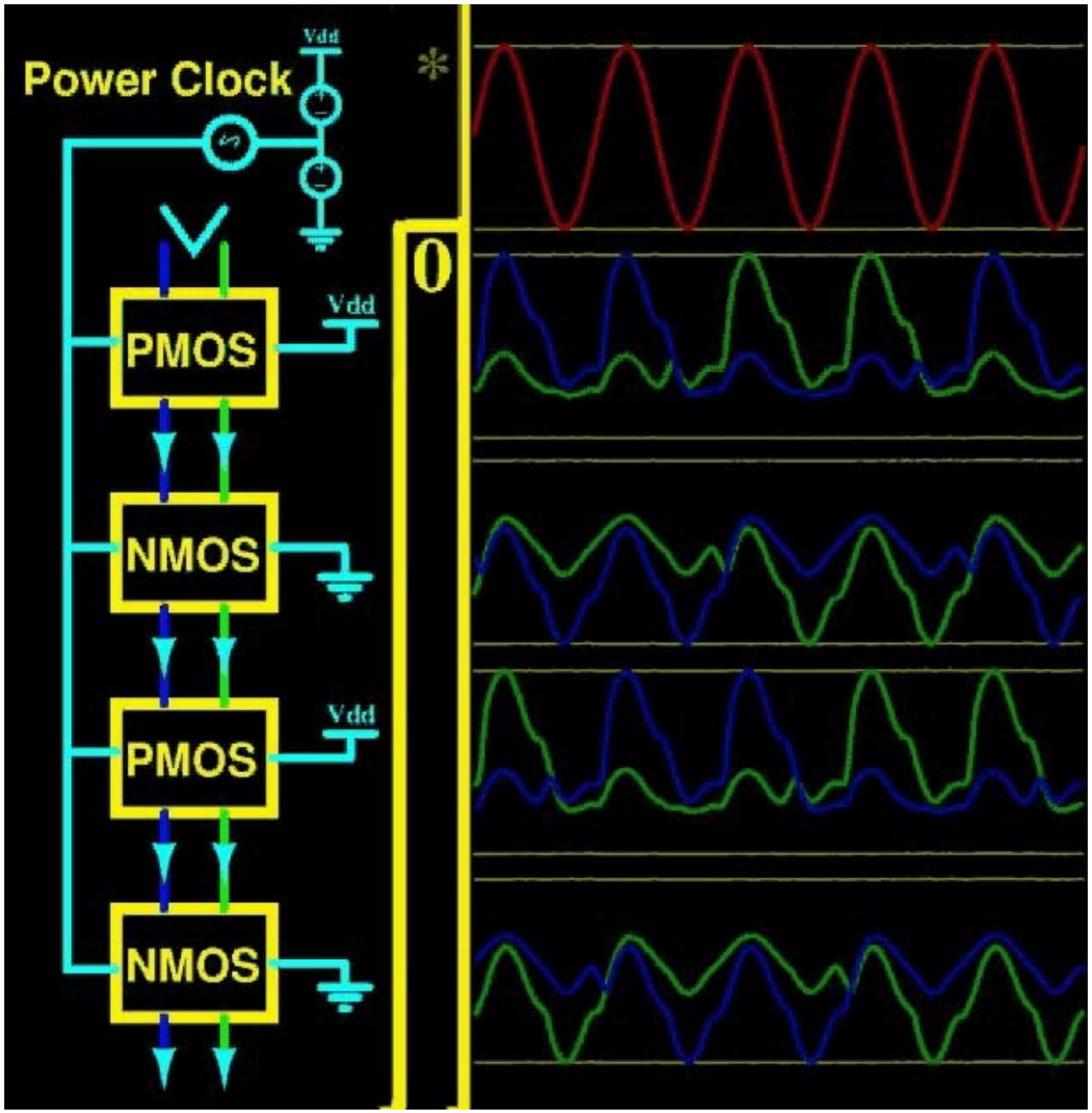


NMOS NAND gate

- Sense amplifier
- Precharge diodes
- Current switches
- Evaluation tree
- Current tail
- Power clock

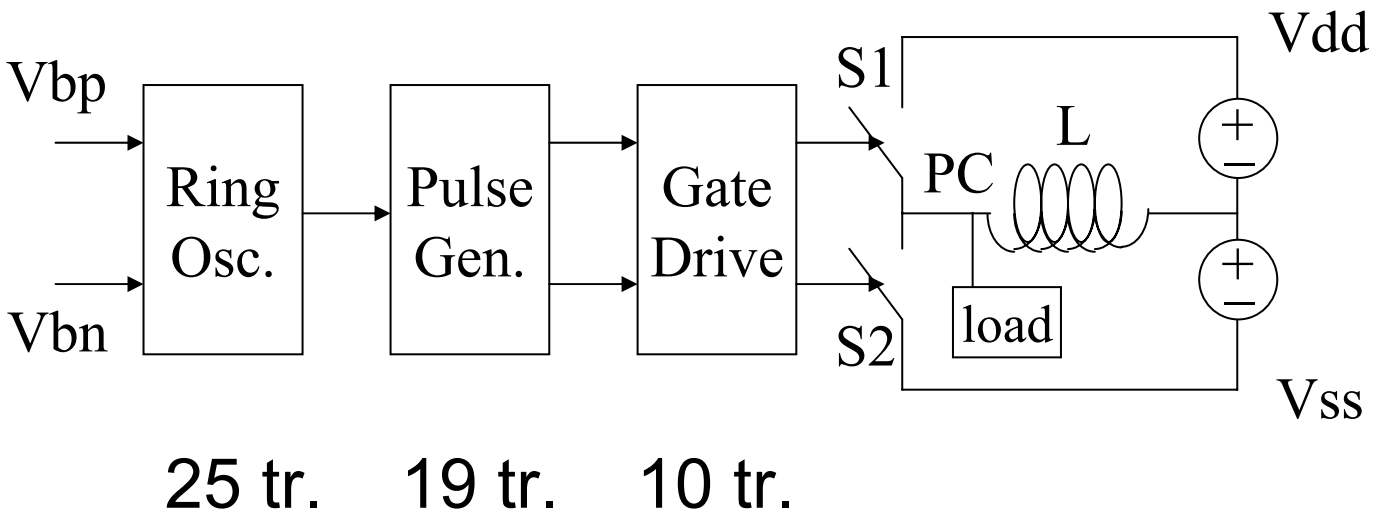
- Single-phase sinusoidal power-clock
- Minimum-size evaluation tree
- Dual-rail noise-tolerant design
- Balanced clock load

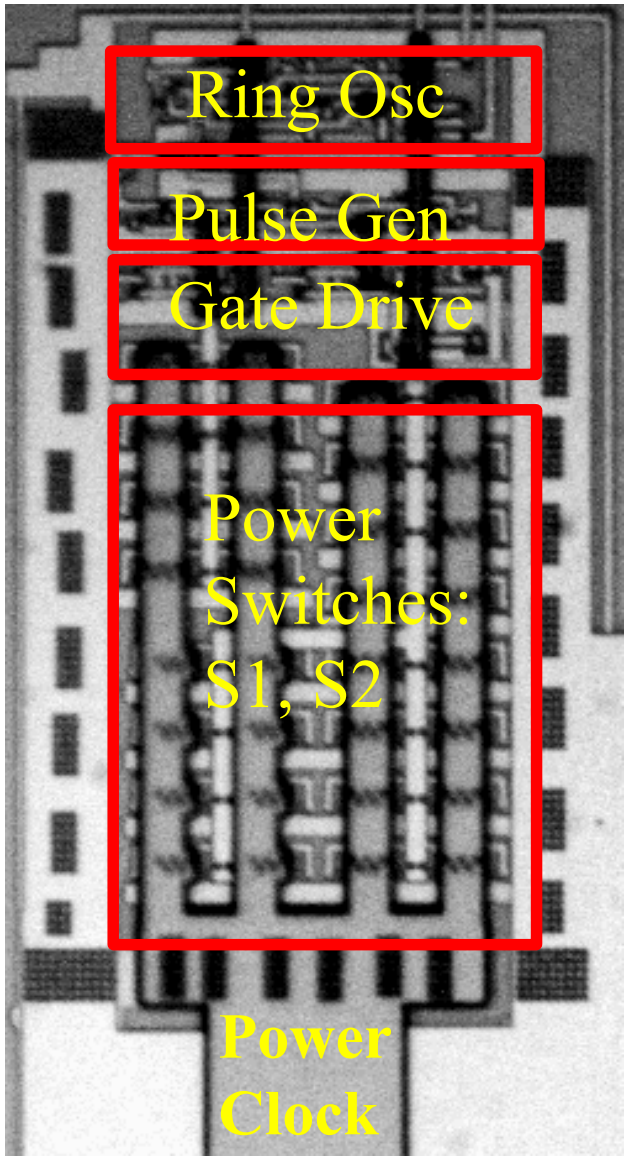
Cascade Operation



- NMOS and PMOS gates are cascaded like domino logic.
- Animation shows tokens propagating through buffer chain.

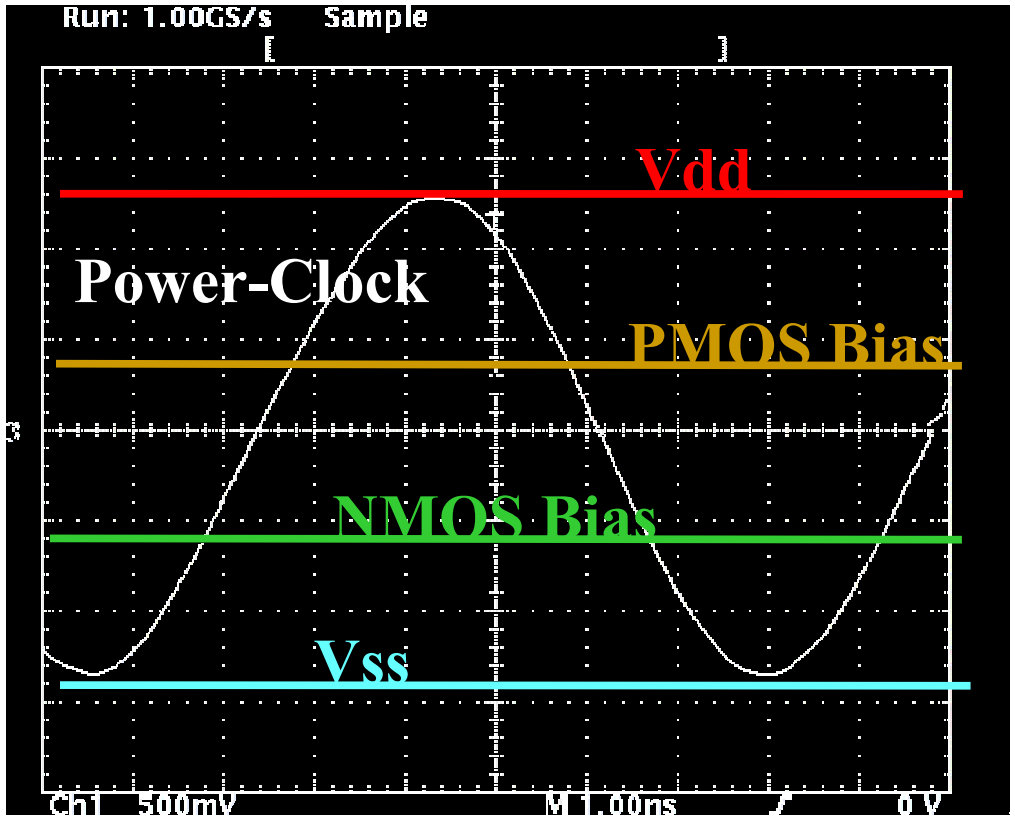
Single-Phase Power-Clock Generator





- Zero-voltage switching
- LC-resonant clock generation
- External/bondwire inductor L
- Resistive/capacitive load
- Compact: 170 x 115 μm

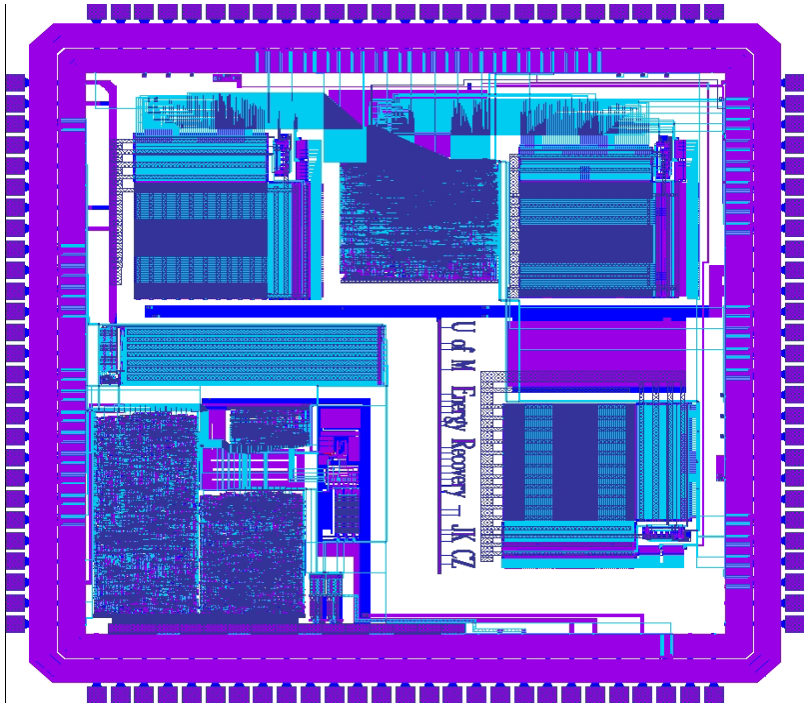
Power-Clock Waveform



- Single-phase sinusoidal waveform @140MHz
- ~60pF load, ~10nH external inductor
- One DC supply (Vdd, Vss), two DC biases (NMOS, PMOS)

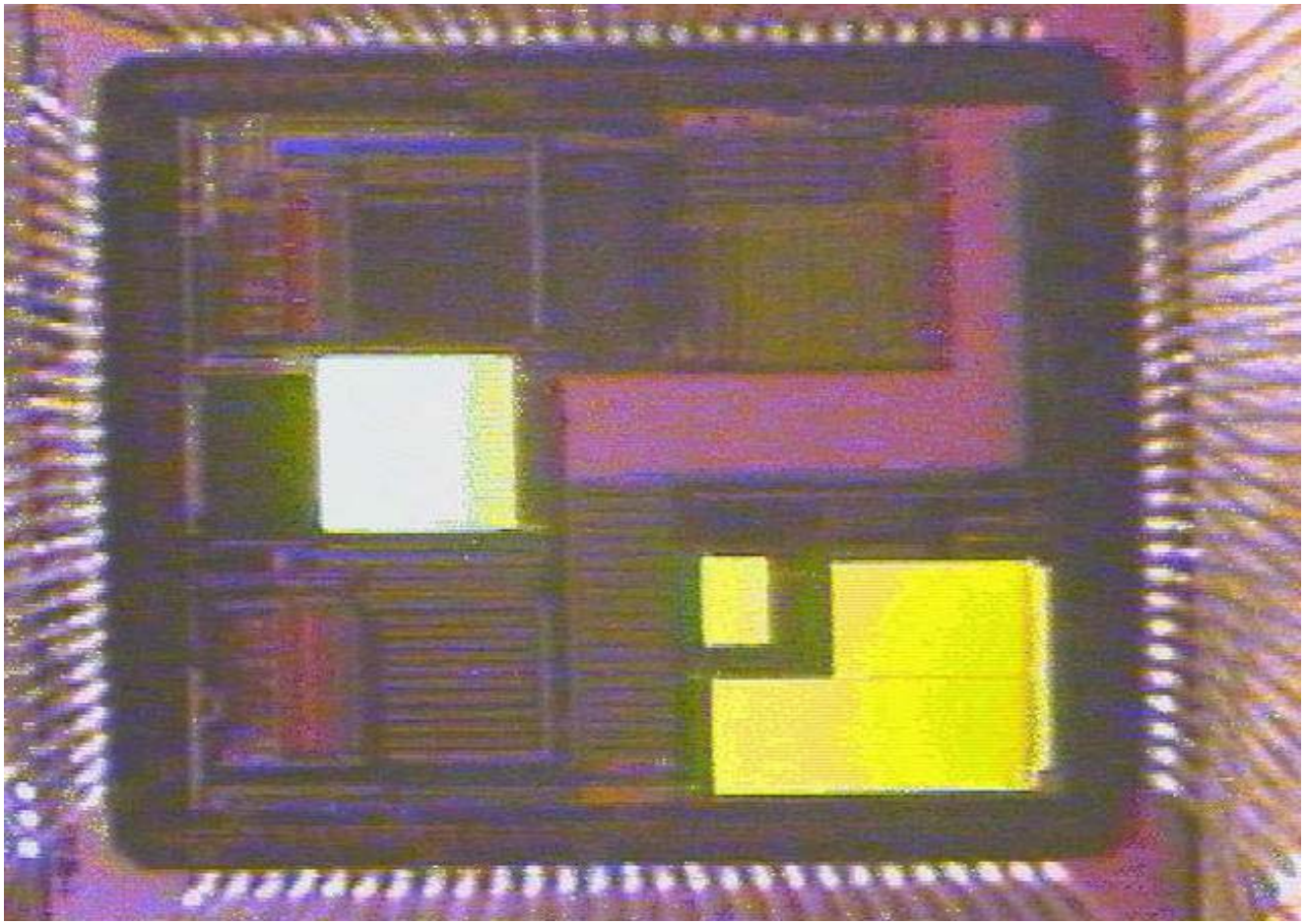
Resonant Clock ASIC

- Compatible with ASIC flow
- Synthesized by Conrad Ziesler and Joohee Kim using in-house standard-cell library and commercial tools
- Energy recovering clock tree and SRAM word/bit lines

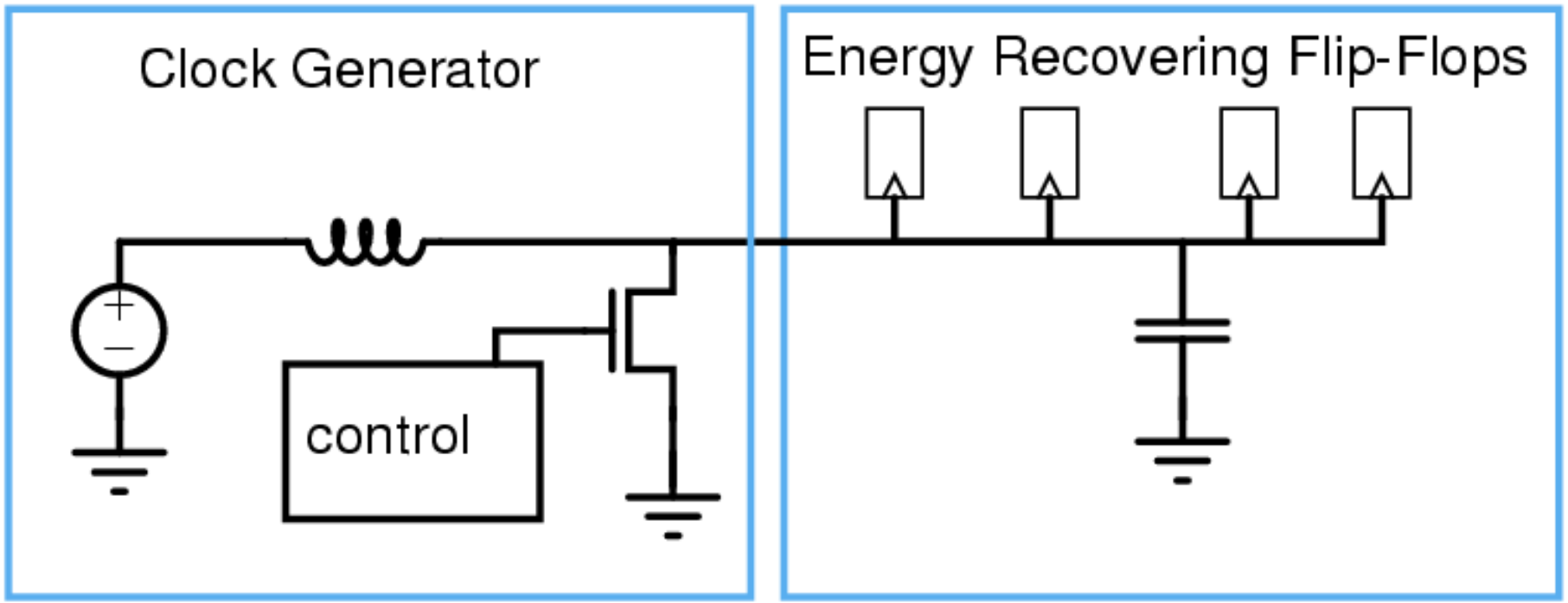


- Low-cost bulk CMOS process: TSMC 0.25µm, 108-pin PGA package, through MOSIS
- High frequency (300MHz)
- Low voltage (1.0-1.5V)

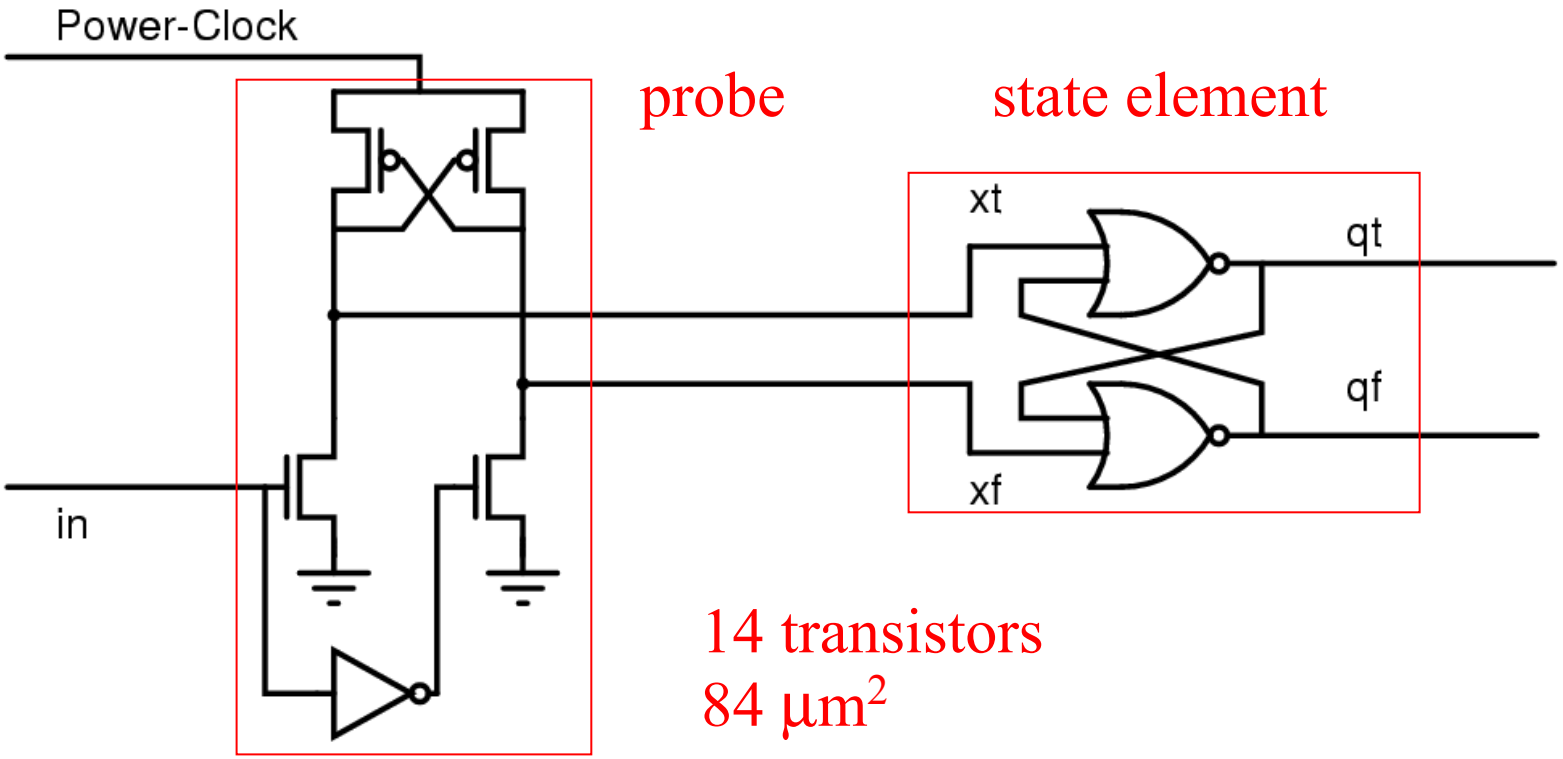
Chip Microphotograph



System Overview



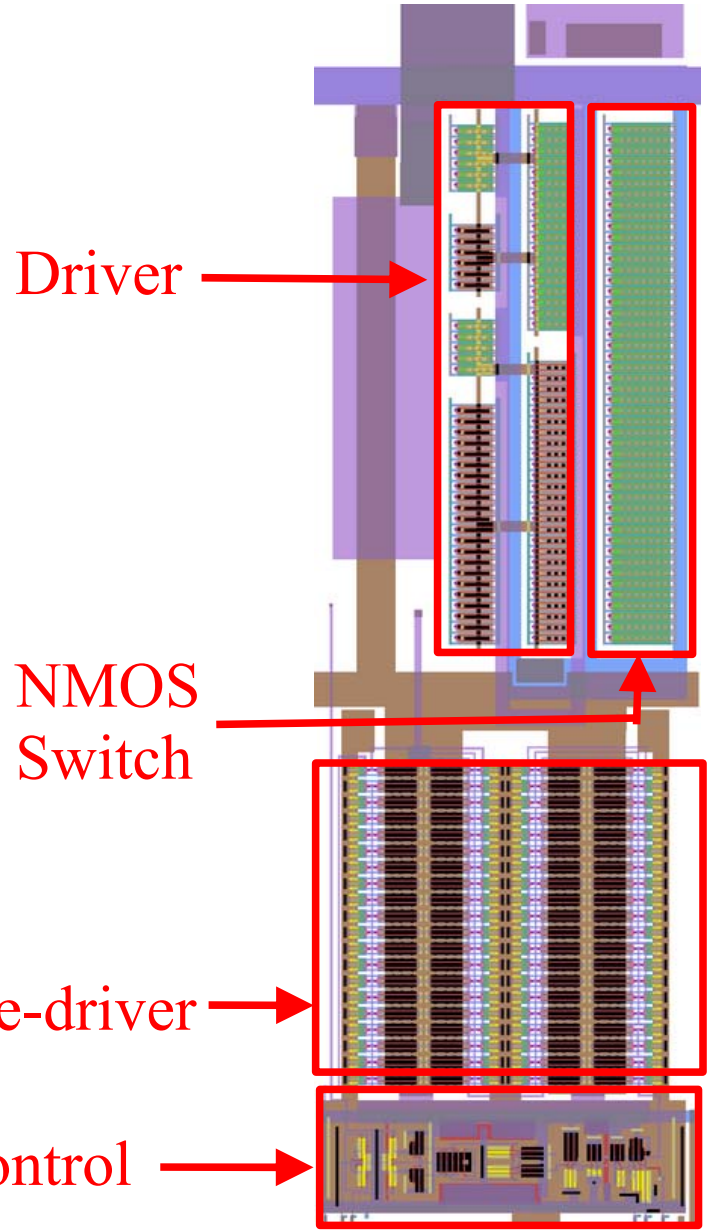
The Energy Recovering Flip-Flop



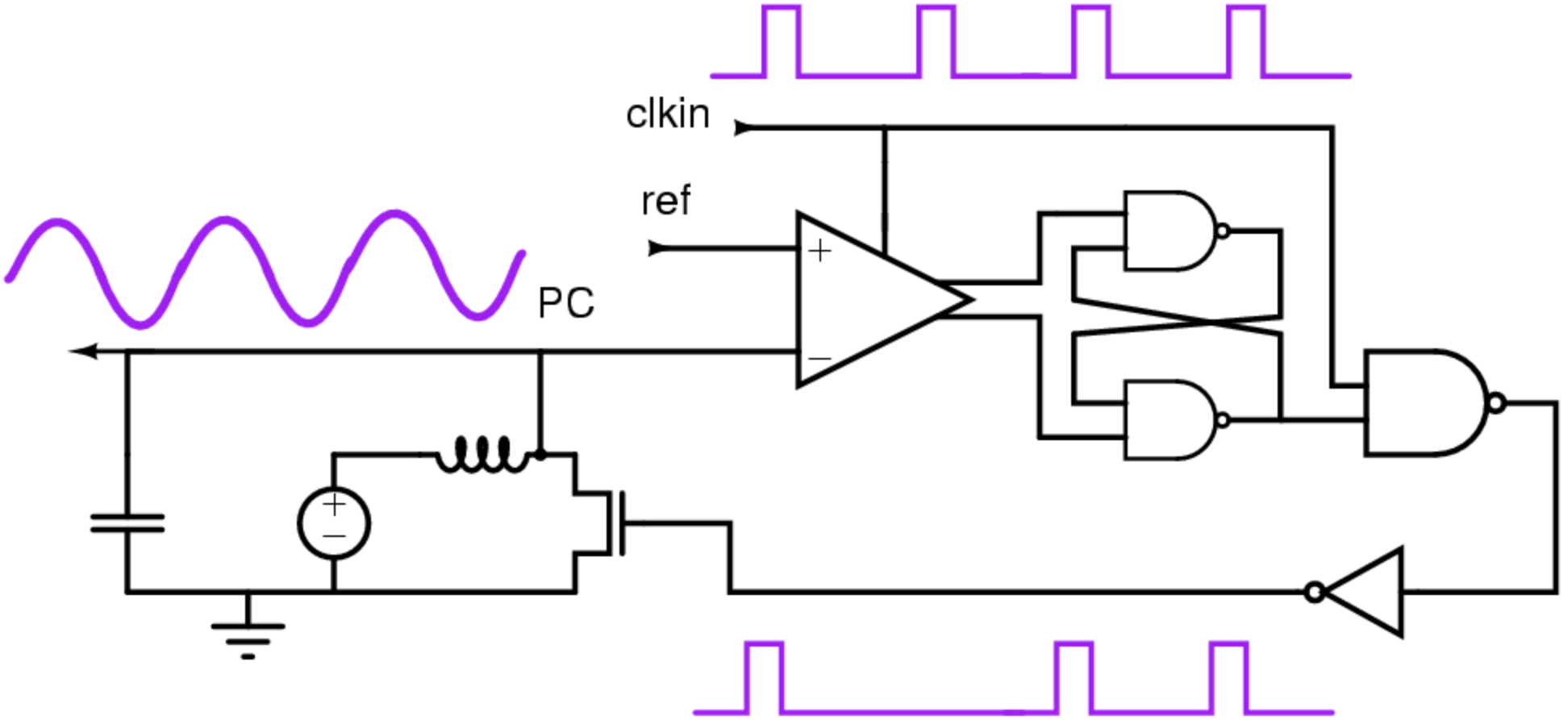
- Clock signal: Single-phase resonant sinusoid
- Probe activates state element only if next state differs from present state.
- Low voltage operation at high speeds
- Delay similar to conventional flip-flops
- Fully compatible with standard-cell ASIC flow

Resonant Clock Generator

- Resonate entire clock capacitance with small inductor
- Pump resonant system with NMOS switch at appropriate times
- NMOS switch only conducts incremental losses whenever “on”

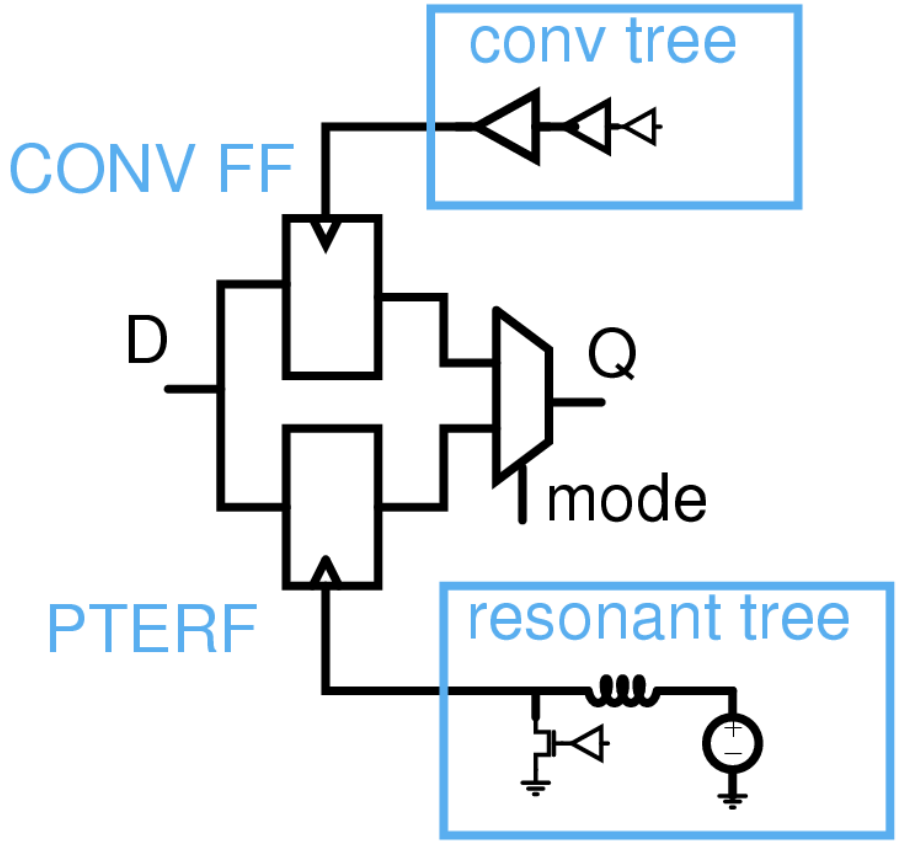


Clock Generator Operation



Recovering vs. Conventional Hardware

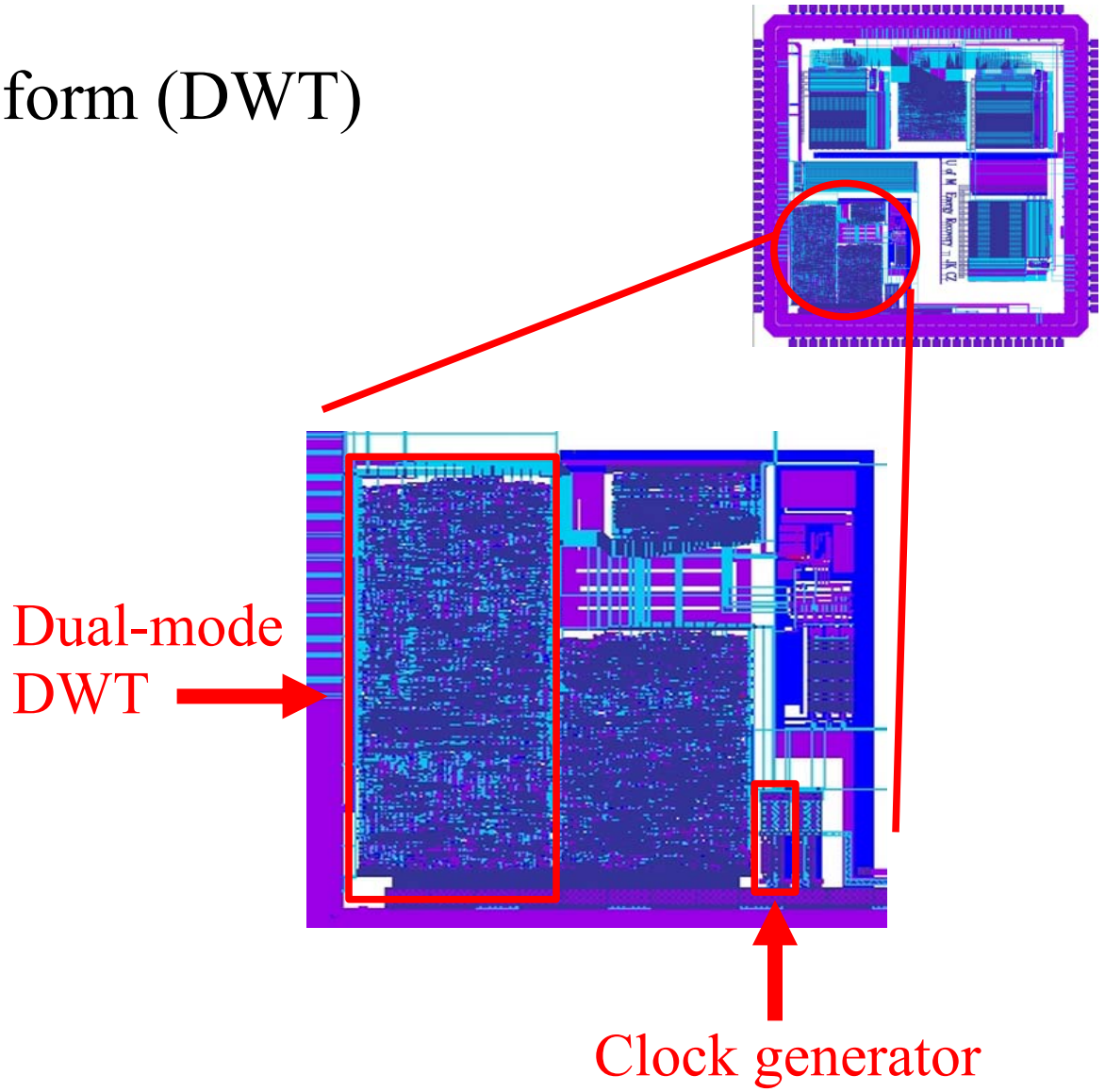
- Synthesized dual-mode ASIC
  - conventional
  - charge recovery
- Dual-mode flip-flop cell
- Conventional clock tree with conventional flip-flop
- Resonant clock tree with energy-recovering flip-flop



- Direct comparison of dissipation at target throughput using identical hardware structures

ASIC Statistics

- Discrete wavelet transform (DWT)
- 3,897 gates, 413 ffs
- 15,571 transistors
- 400µm x 900µm
- 13.6 pF , 21 nH
- 300 MHz , 1.5V
- 0.25µm logic process



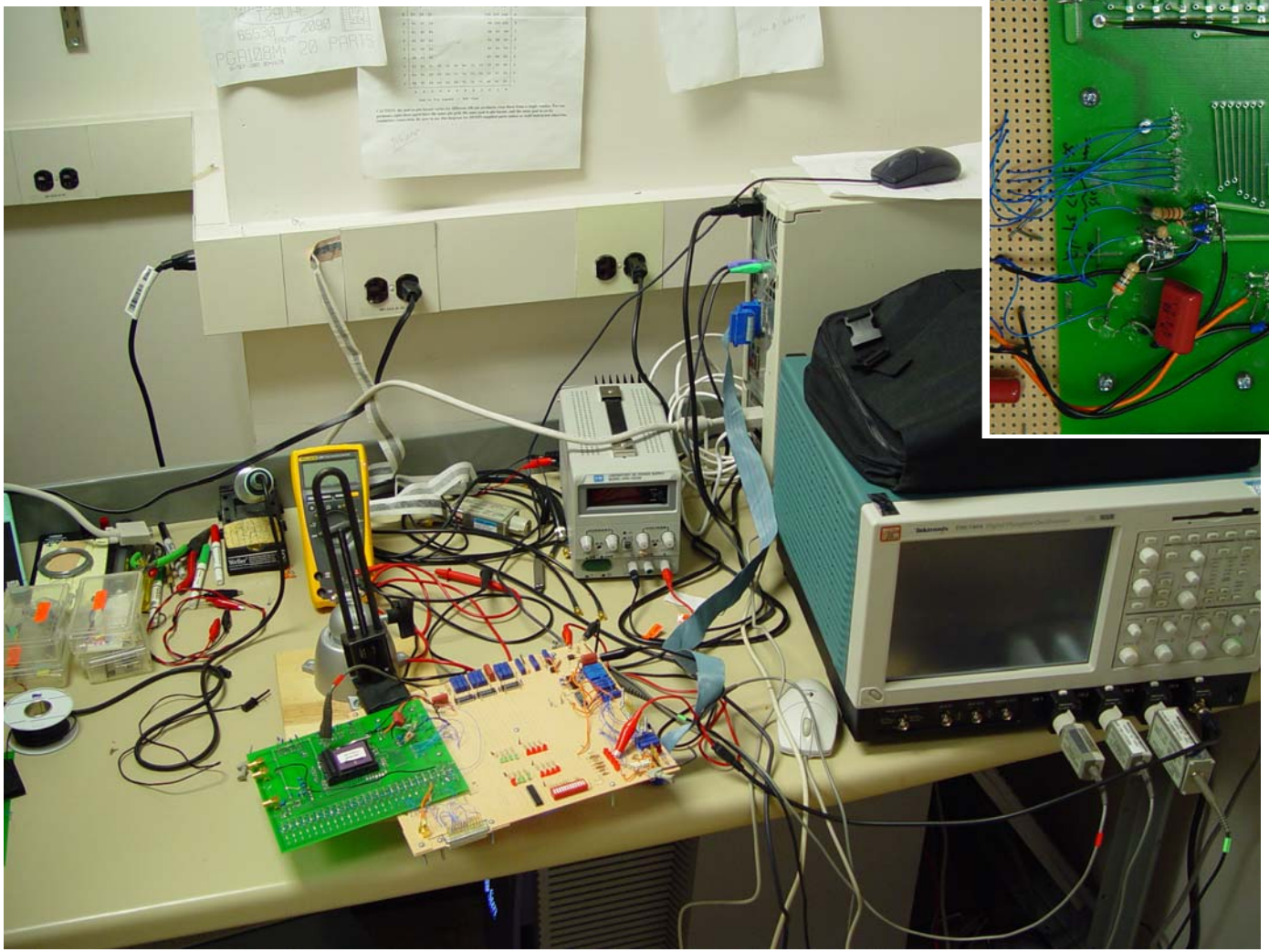
Simulation Results

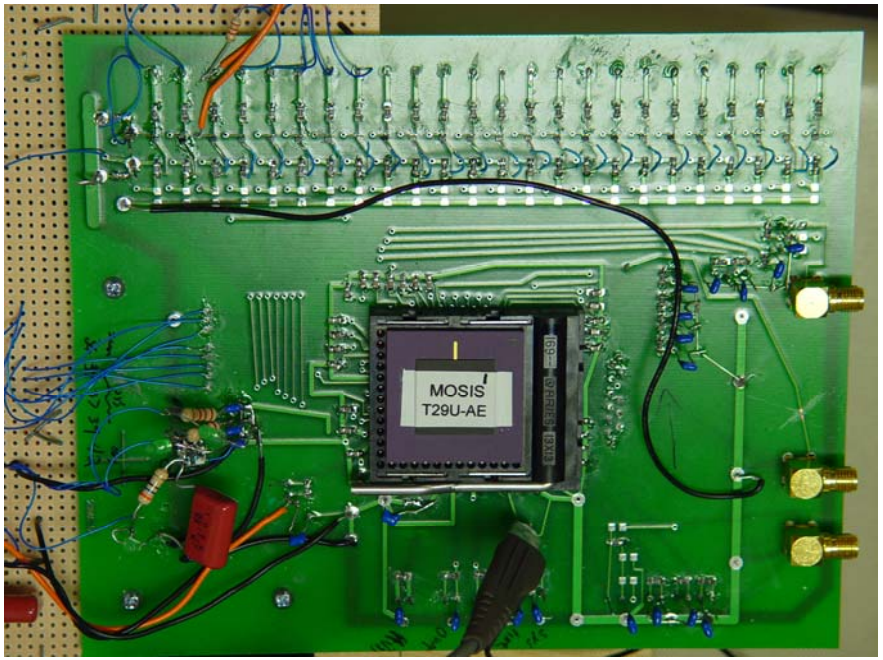
	Per-Cycle Energy Dissipation	
300MHz , 1.5V	Charge Recovery	Conventional
Idle	6.74pJ	29.72pJ
Active	68.47pJ	78.28pJ

Total system dissipation

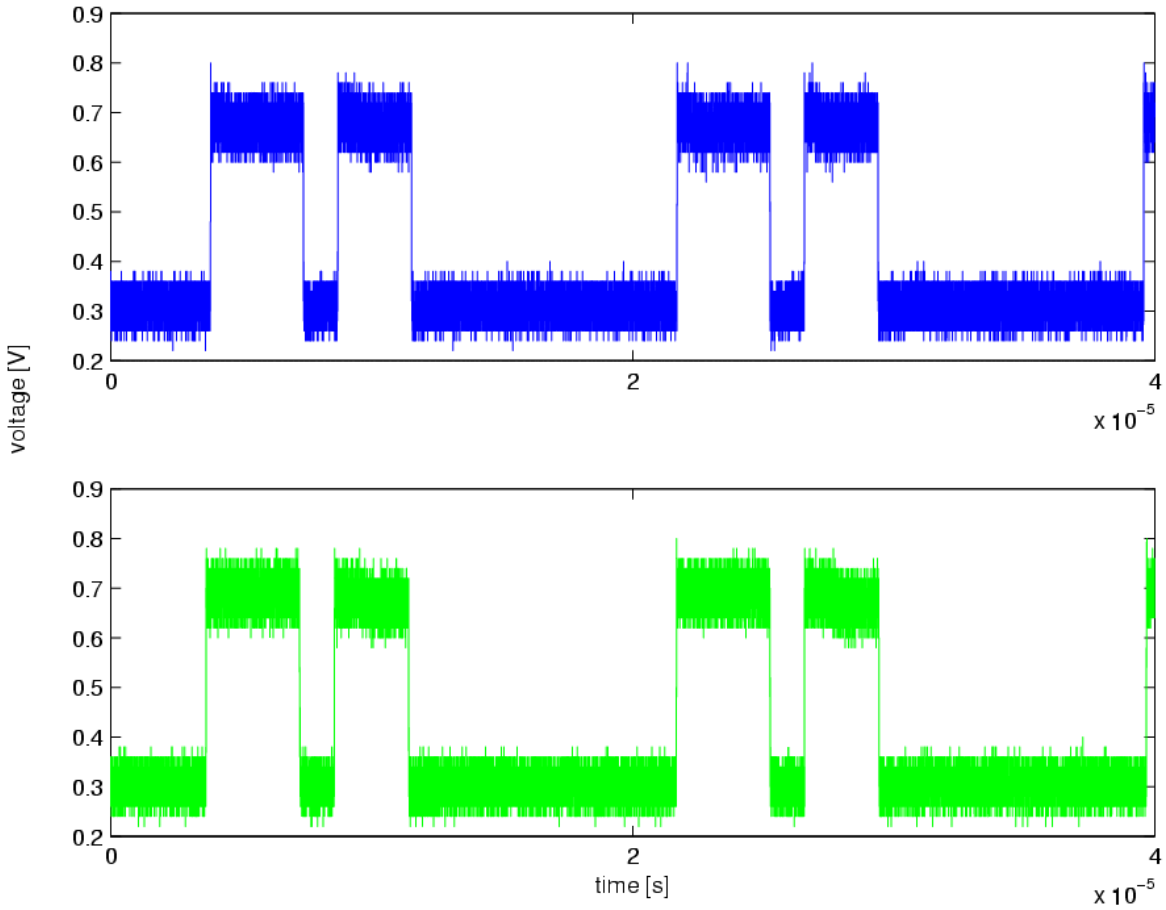
- Conventional mode includes clock tree
- Energy recovery mode includes on-chip clock generator

Lab Setup





Correct Function



signature output (conventional)

signature output (energy recovery)

- 115MHz
- 5nH high-Q external inductor

Power Measurements I: Packaged Die

115MHz , 1.5V	Charge Recovery	Conventional
Idle	2.6mW	4.3mW
Active	8.9mW	11.7mW

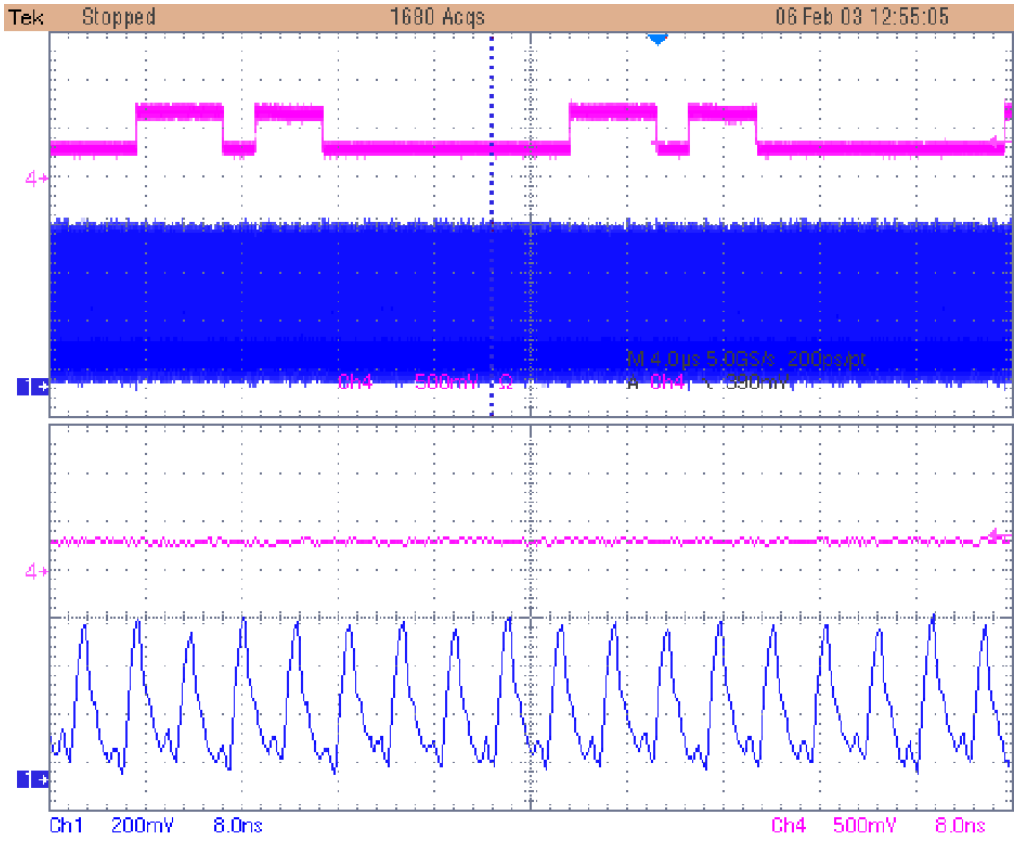
- Total system measurements by monitoring DC supplies
  - Conventional mode includes clock tree
  - Energy recovery mode includes on-chip clock generator
- Not included: I/O supply, test circuitry, ring oscillator
- Energy recovery data is *conservative* (obtained when simultaneously driving two DWT cores, one always in idle)

Self-Resonance at 225MHz

200,000 samples
@200ps intervals

4µs/div

8ns/div



signature output
(energy recovery)

buffered
power clock

- No external inductor!
- Clock resonates using parasitic inductance of package
- Lossy parasitics limit power savings

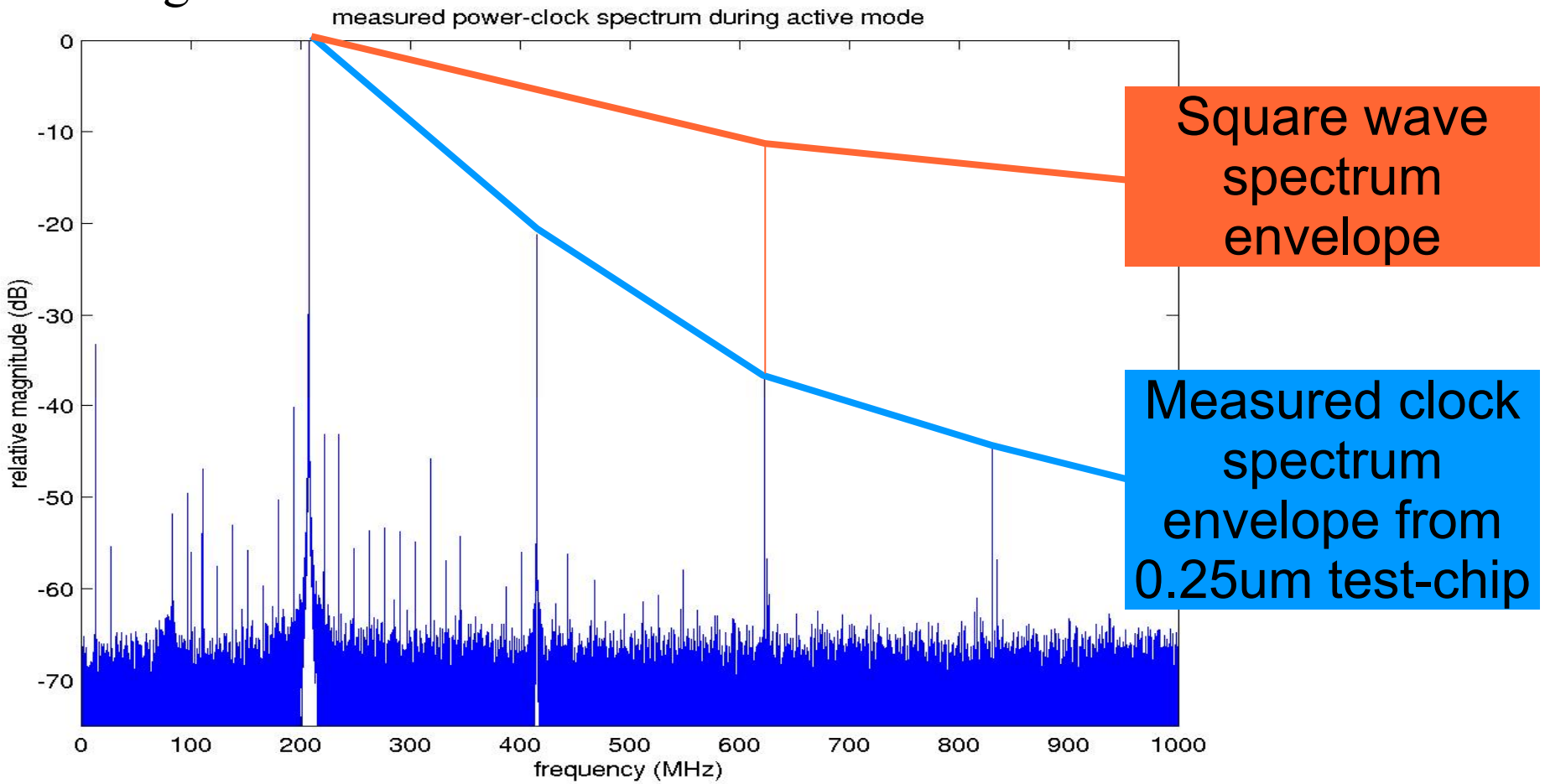
Power Measurements II: Bare Die

200MHz , 1.3V	ASIC Power	
Idle	4.6mW	(57% measured power savings)
Active	15.0mW	(25% measured power savings)

- Energy recovering clock-tree and flip-flops
- Total system measurements by monitoring DC supplies
  - Conventional mode includes clock tree
  - Energy recovery mode includes on-chip clock generator
- Unpackaged die, 4.2nH off-chip inductor
- Not included: I/O supply, test circuitry, ring oscillator
- Measured design was largely *unoptimized*.

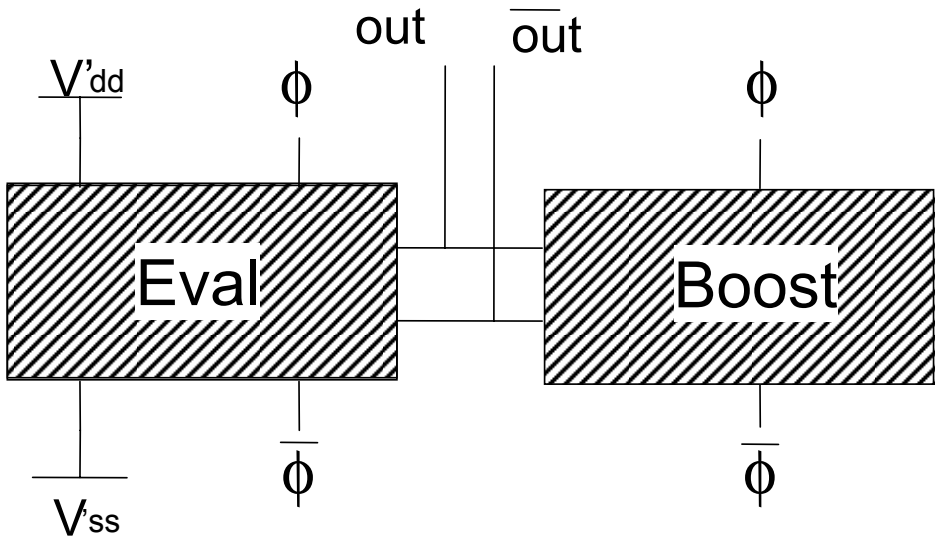
Beyond Low Power: Low EMI

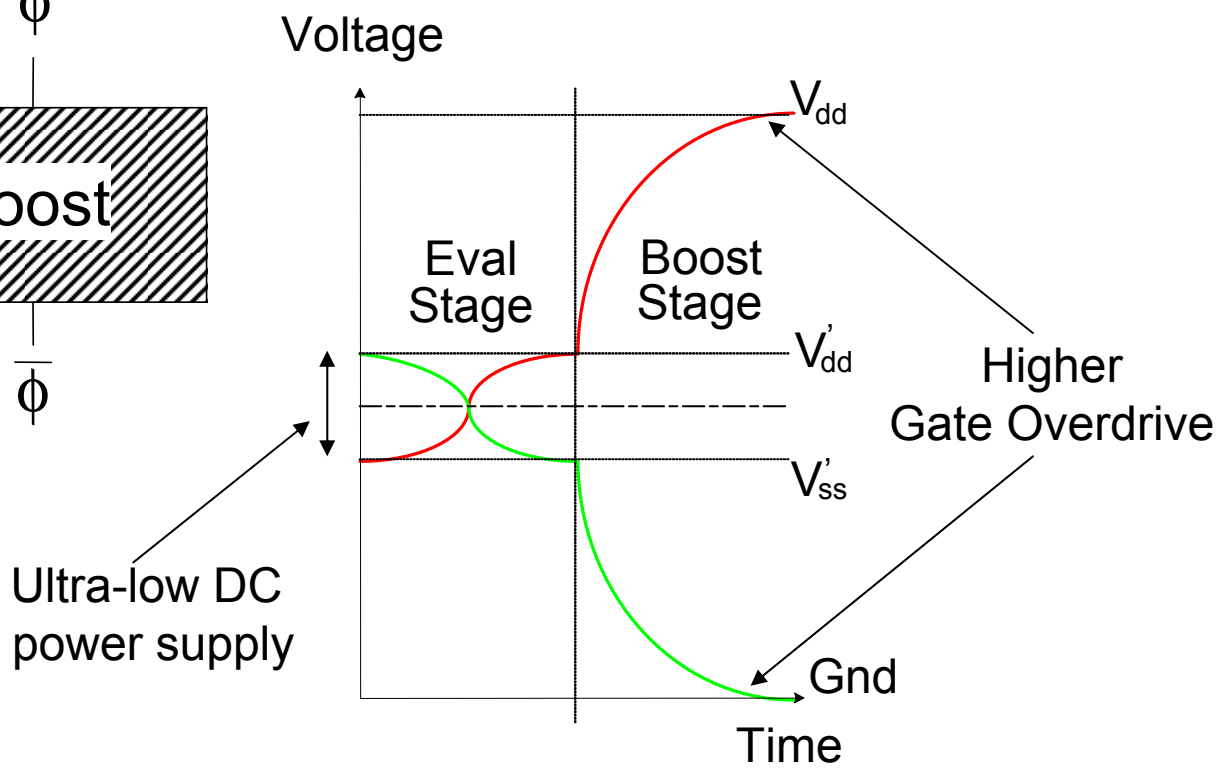
- Smooth waveforms yield simpler spectrum with suppressed high-frequency harmonics
- Potentially key advantage for next-generation mixed digital / RF designs



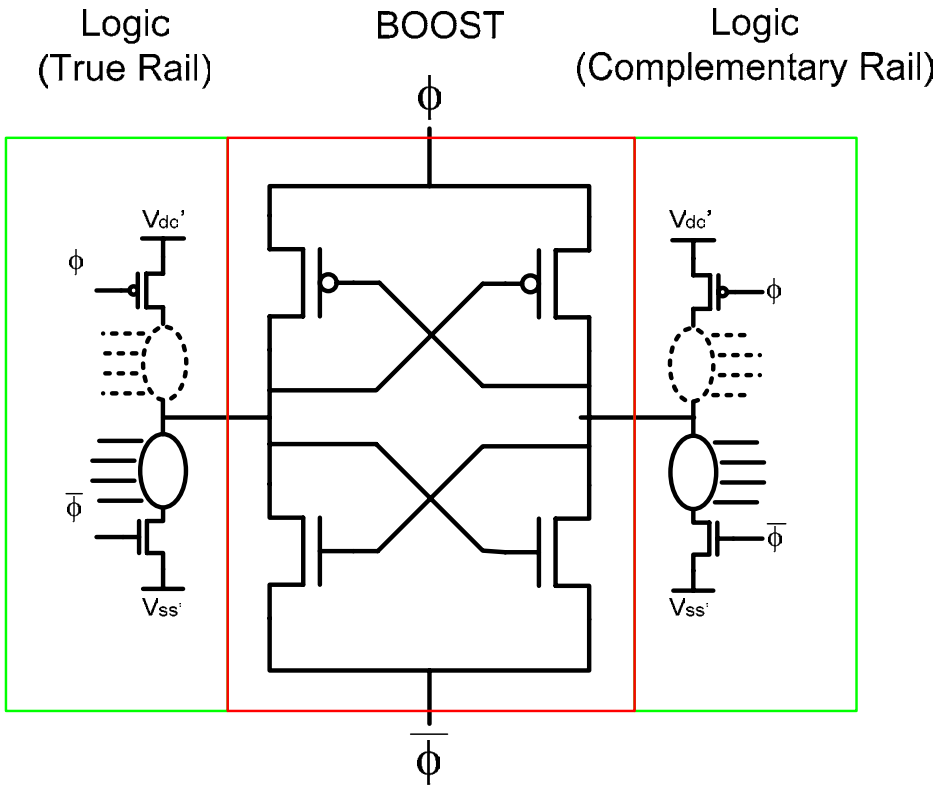
GHz-Class Charge Recovery: Boost Logic

- Conventional logic evaluation stage with ultra-low DC supply
- Evaluation devices operating in super-threshold linear mode
- Charge recovery level conversion ("Boost") stage overdrives next gate
- "Boost" spread over time, trading off latency for efficiency



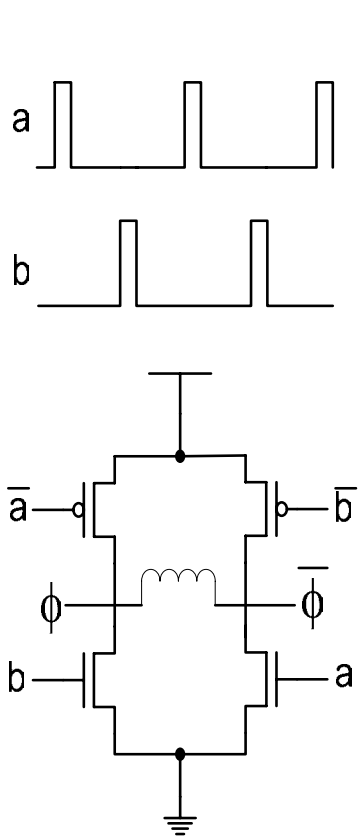


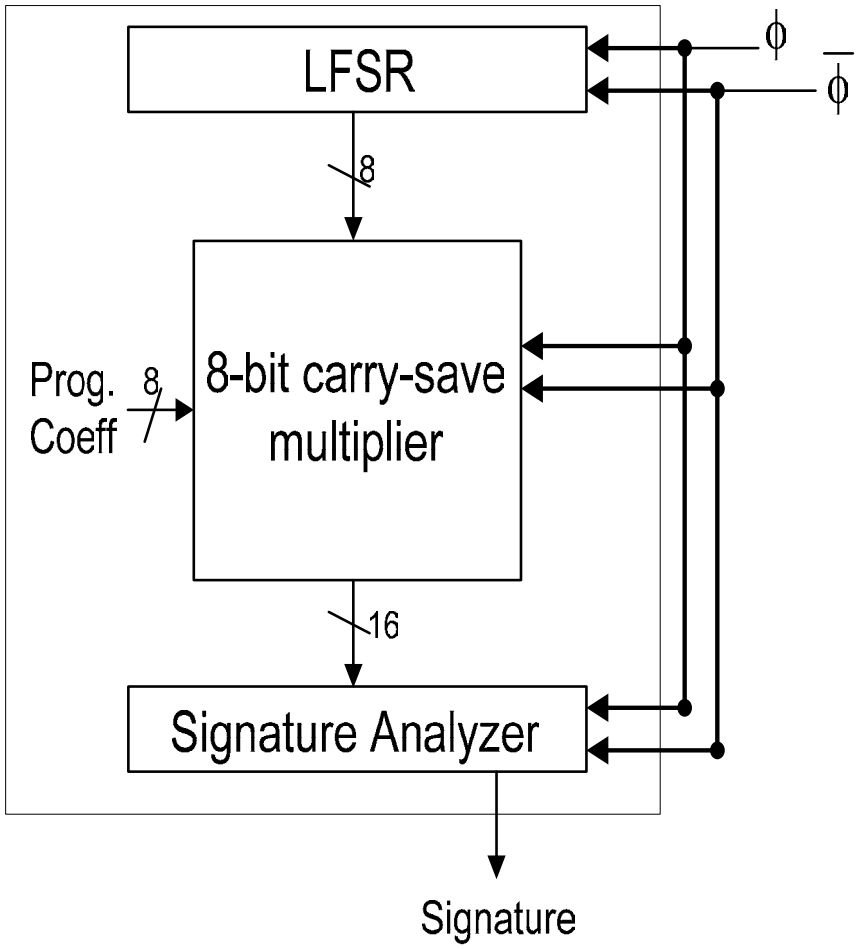
Boost Logic Structure



- Data independent capacitance presented to clock tree
- Pre-resolved sense-amplifier
- Boost stage is timing element; no throughput penalty
- Less sensitive to power supply variation (devices operating in linear mode)
- pMOS evaluation tree not required

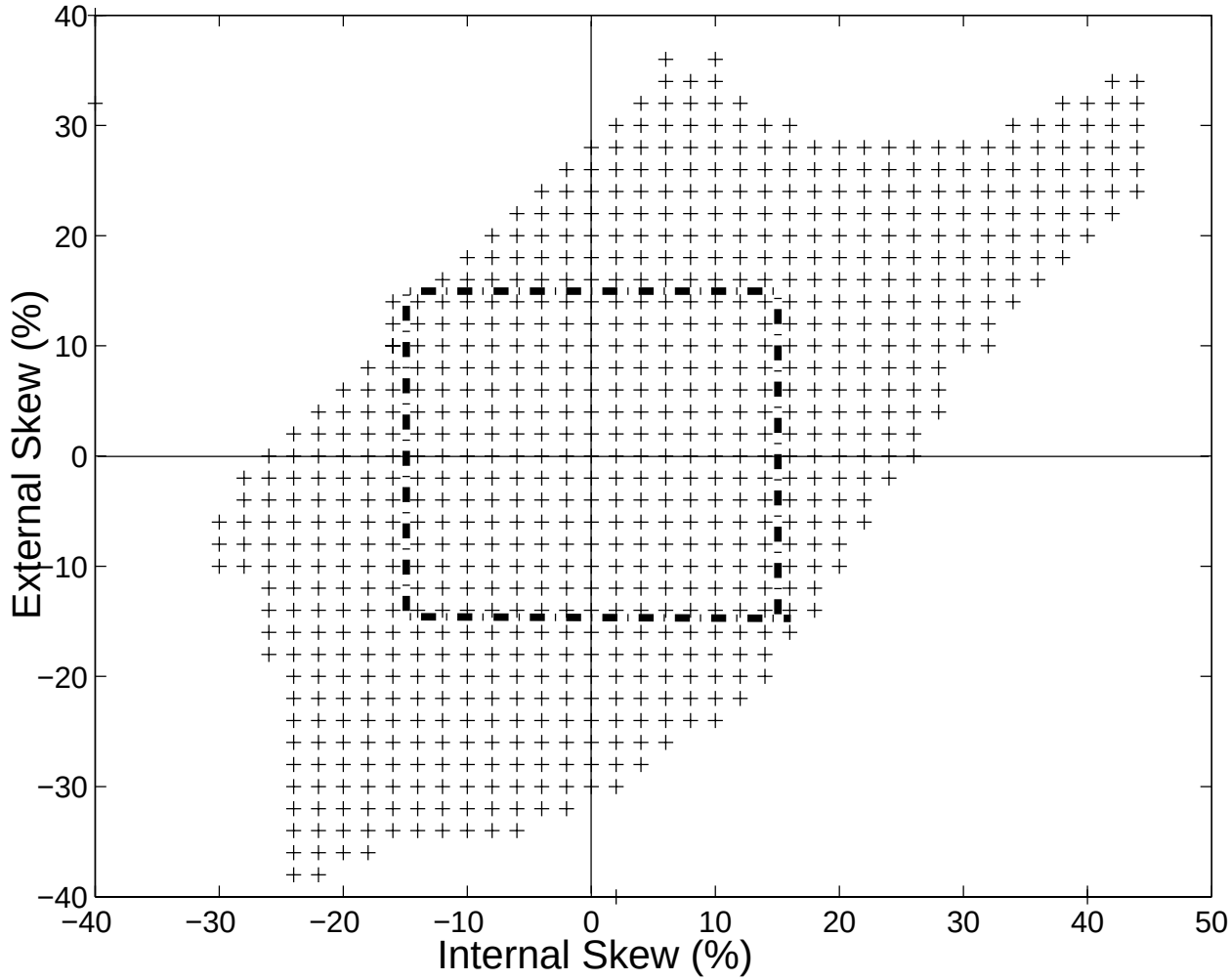
8-bit Carry-Save Multiplier





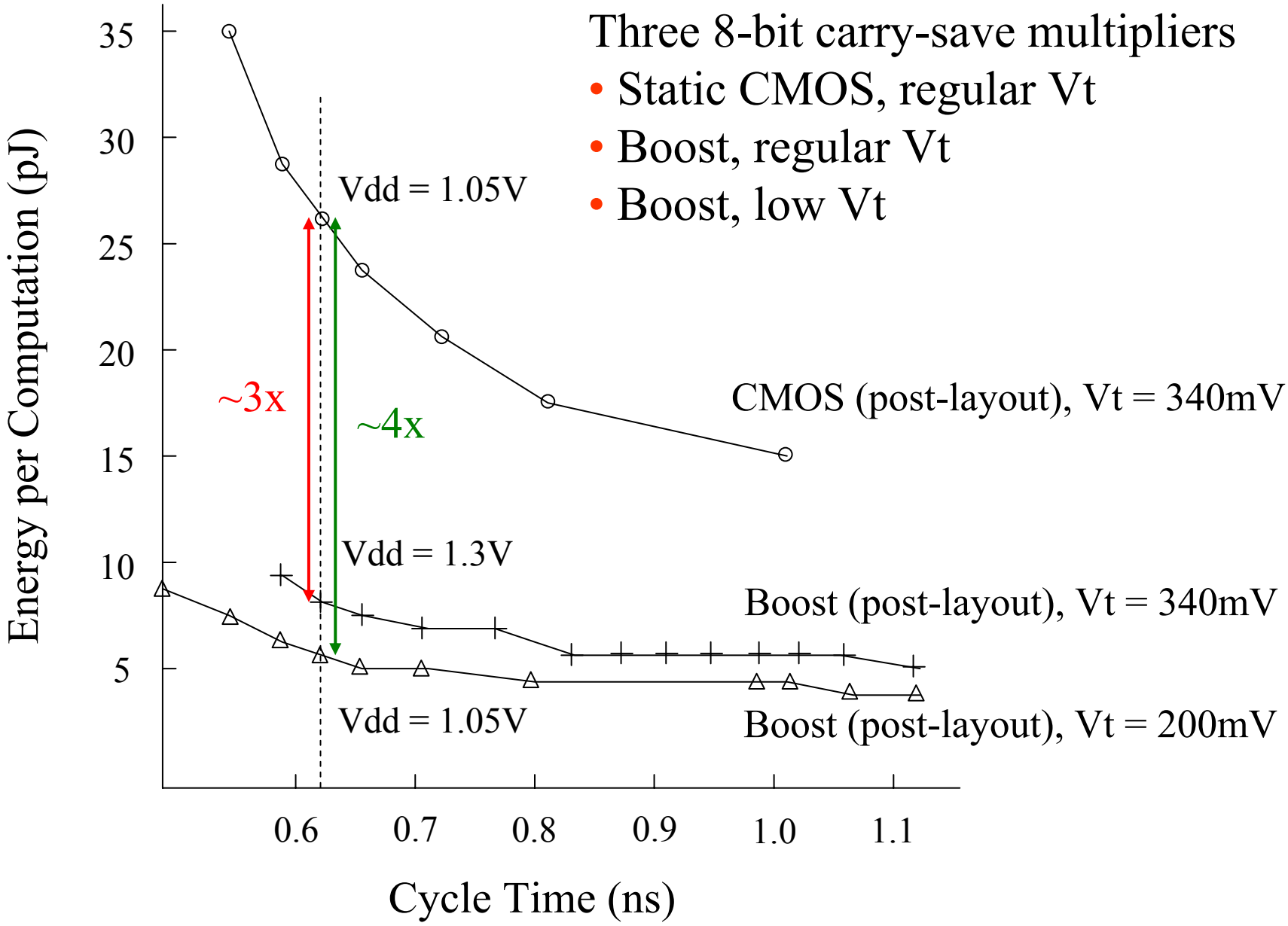
- LFSR and Signature Analyzer both implemented in Boost
- H-Bridge clock generator topology
- 13-element on-chip inductor model used in simulations

Clock Skew Tolerance



- ±15% tolerance to simultaneous clock skew

Boost vs Conventional Multiplier



Conclusion

- Working silicon that realizes the potential of charge recovery
  - power savings over conventional CMOS
  - operating speeds all the way to 1GHz
  - low control and hardware overhead
  - integrated power-clock generators
- Multiplier chip in 0.5µm CMOS
  - Fine-grain recovery at the level of individual gate outputs
  - True singe-phase energy recovering dynamic logic
  - 2—4x energy savings over static CMOS in 50—200MHz
- DWT chip in 0.25µm CMOS
  - ASIC-compatible design flow
  - Correct operation up to 300MHz
  - Dual-mode chip for direct hardware comparison:
    - 60—75% of conventional power dissipation at 115MHz (packaged die)
    - 43—75% of conventional power dissipation at 200MHz (bare die)
- Dynamic adder in 0.13µm CMOS
  - Fine-grain recovery at gate outputs, trading off latency for efficiency
  - Correct operation up to 1GHz
  - 3—4x energy savings over conventional design at GHz-class speeds

Links and Acknowledgments

Web Sites

http://www.eecs.umich.edu/acal/energyrecovery

http://www.eecs.umich.edu/acal/adiabatic/

Energy recovery group

Suhwan Kim (emeritus)

Joohee Kim

Visvesh Sathe

Jae-Sun Seo

Conrad Ziesler (emeritus)

Juang-Ying Chueh

Sujay Phadke

Funded in part by ARO and DARPA

DAAG-55-97-1-0250, DAAD-19-99-1-0340, DAAD-19-03-1-0122, N66001-02-C-8059