Localized Synthesis, Assembly and Integration of Silicon Nanowires

by

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Abstract

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Localized synthesis, assembly and integration of one-dimensional silicon nanowires with MEMS structures is demonstrated and characterized in terms of local synthesis processes, electric-field assisted self-assembly, and a proof-of-concept nanoelectromechanical system (NEMS) demonstration. Emphasis is placed on the ease of integration, process control strategies, characterization techniques and the pursuit of integrated devices.

A top-down followed by a bottom-up integration approach is utilized. Simple MEMS heater structures are utilized as the microscale platforms for the localized, bottom-up synthesis of one-dimensional nanostructures. Localized heating confines the high temperature region permitting only localized nanostructure synthesis and allowing the surroundings to remain at room temperature thus enabling CMOS compatible post-processing. The vapor-liquid-solid (VLS) process in the presence of a catalytic nanoparticle, a vapor phase reactant, and a specific temperature environment is successfully employed locally. Experimentally, a 5nm thick gold-palladium layer is used as the catalyst while silane is the vapor phase reactant. The current-voltage behavior of the MEMS structures can be correlated to the

approximate temperature range required for the VLS reaction to take place. Silicon nanowires averaging 45nm in diameter and up to 29μm in length synthesized at growth rates of up to 1.5μm/min result.

By placing two MEMS structures in close proximity, 4-10μm apart, localized silicon nanowire growth can be used to link together MEMS structures to yield a two-terminal, self-assembled micro-to-nano system. Here, one MEMS structure is designated as the hot growth structure while a nearby structure is designated as the cold secondary structure, whose role is to provide a natural stopping point for the VLS reaction. The application of a localized electric-field, 5 to 13V/μm in strength, during the synthesis process, has been shown to improve nanowire organization, alignment, and assembly.

The integrated nanoelectromechanical system was found to be mechanically resilient as it proved to successfully withstand a wide variety of post-processing steps, including manipulations and examinations under scanning and transmission electron microscopes and aqueous processing, although a super critical drying step is necessary to preserve the integrated system during the drying process. Electrical characterization of the system proved challenging due to low carrier concentration and possible transport issues at the nano-micro interface. Nonetheless, in a proof-of-concept demonstration, the system was functionalized and tested for a hydrogen sensing application.

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Professor Liwei Lin, Chair Date

Dedication

To my parents

Acknowledgments

I wish to thank Professor Liwei Lin for advising and mentoring me through my graduate education. I sincerely appreciate the 'big picture view', the brainstorming sessions and the ongoing encouragement. The nature of this dissertation provided me with the opportunity to start on a new and unique path, and I know I greatly benefited from this experience. I acknowledge Prof. Lin for believing that I can make this happen.

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I would also like to acknowledge Ron Wilson for first introducing me to the

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Finally, I wish to thank the Nanotechnology Fellowship from the State of California and the COINS program for supporting my graduate education and providing the foundation for a multidisciplinary nanoscale research environment.

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1 Introduction

1.1 Scope of Work

This dissertation focuses on the utilization of one-dimensional nanostructures as building blocks in the fabrication of hybrid micro-nano-self-assembled systems. More specifically, a process for the direct integration of silicon nanowires with MEMS structures to yield a two-terminal system is developed and its attributes are explored. The goal is to develop a controlled fabrication technique that provides an economically sound process, and sets a path for a fully integrated nano-to-micro-to-macro system while maintaining acceptable performance levels. A conceptual view of the micro-to-nano self-assembled system is presented in Figure 1.1.

A product is only as good as its interface with its user and nanoscale devices are no different. In fact, our ability to study and utilize the nanoscale is contingent upon our ability to effectively link nano components with larger scale components. This capability is a key to exploiting the possibilities offered by nanotechnology. This work presents a unique, alternative approach, a counter to current state-of-the-art processes, to realizing the required integration across length scales necessary to produce and interface with nanoscale devices. The advantages and opportunities offered by this strategic combination of bottom-up and top-down fabrication techniques while eliminating high-cost, low-yield integration processes and enabling

on-chip integration and CMOS compatibility are explored.

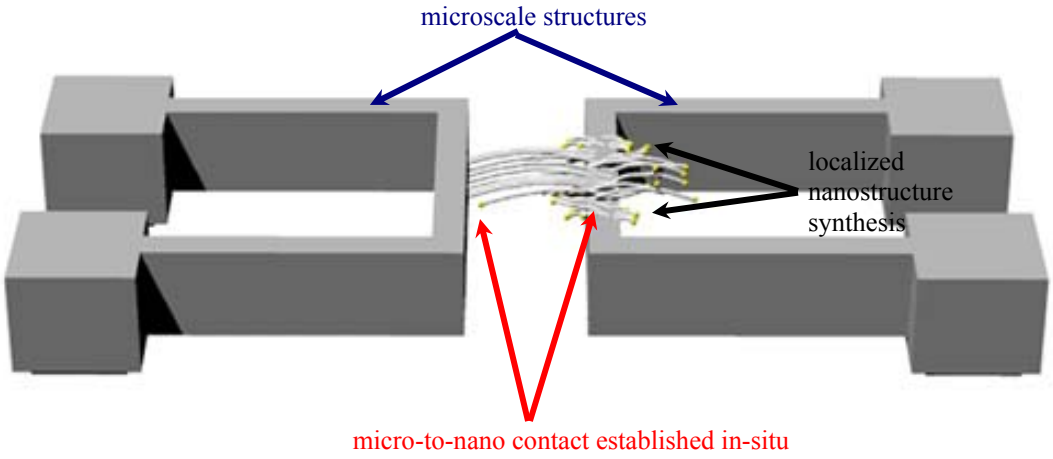

Figure 1.1. Conceptual view of the micro-to-nano integrated system realized through the localized synthesis and self-assembly of silicon nanowires.

This work focuses on silicon nanowires as the capability to controllably shrink silicon based devices is an attractive path and a basic need facing the IC sector. Familiarity with silicon's behavior and its compatibility with a wide range of standard processes further make it a relevant choice. It is important to remember that the approach and methodology described in this work are not limited to silicon nanowires and may in fact prove be better suited for other nanomaterials. This work fits well within the grand vision for nanotechnology and the specifically ongoing efforts focused on developing a fully integrated nanoscale sensor with on-chip microscale power source, controls and electronics as illustrated by the schematic in Figure 1.2. While the fabrication and operation of the components in quadrants II, III and IV have been widely demonstrated, both as individual components and as integrated

devices, this work explores the feasibility of developing a compatible process for fabricating and defining the infrastructure for the addition of a nanoscale sensor in quadrant I.

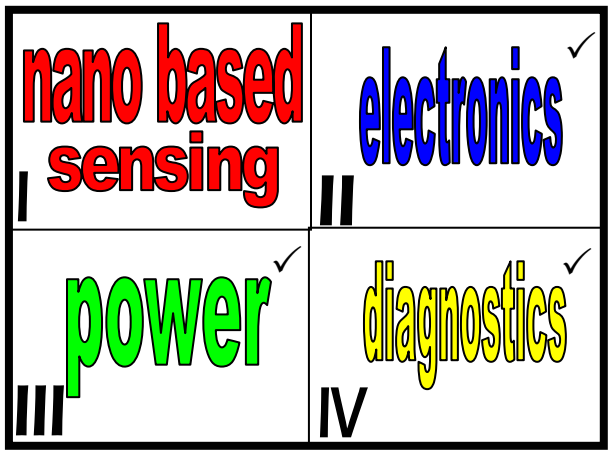

Figure 1.2. Motivational vision: introducing and assessing the feasibility of a direct nano-to-micro integration method to enable a manufacturable and cost effective process for merging nano-based applications with existing technologies.

Chapter 1 introduces 1-dimensional nanostructures and examines current important considerations for the developing technology while Chapter 2 examines the literature with respect to one-dimensional nanostructure synthesis, control, as well as assembly and integration techniques. Chapter 3 presents the alternative approach to nanoscale integration and examines the strategic combination between bottom-up and top-down techniques while Chapter 4 offers methods for assembly as well as enhanced control and ordering. Chapter 5 focuses on various characterization efforts of the system and its components and presents a basic device application. Finally, Chapter 6 offers concluding remarks and presents opportunities for future work.

1.2 Nanotechnology Today

World-wide, nanoscale research and development efforts are abundant and span the wide scope of interrelated fields offered at this scale, from biology to quantum physics. The nanotechnology focus spans academia, industry and government efforts. These research efforts have contributed to a number of nano-based products as well as the establishment of a large number of start-up companies focusing on specific nano-based applications. Nanotechnology is unique since for the first time a highly multidisciplinary team approach is required in order to effectively evaluate, tackle and develop its attributes. It is clear that nanotechnology has yet to 'take off' but the next few years promise significant innovation and advancement.

1.2.1 A Niche for 1-Dimensional Nanostructures

One-dimensional nanostructures are a unique set of building blocks, capable of serving as functional components as well as mechanical and, or electrical interconnects. These nanostructures are essentially wires or cylindrically shaped objects where a nanoscale cross section and a microscale length define these high aspect ratio structures. The 1-dimensional designation refers to the restriction on the motion of carriers to a single dimension. A high surface-area-to-volume ratio makes these nanostructures prime candidates for ultra sensitive chemical and biological sensing applications [1]. The fabrication of transistor architectures based on semiconducting nanostructure gates have been demonstrated and suggests a role for these structures in nanoelectronics as well [2]. In addition, the role of these nanostructures in next generation nano-elecromechanical systems (NEMS) appears

promising, as for example nanoresonator applications where the nanostructures serve as nanoscale beams are currently being explored [3]. Finally, the functionality of these nanostructures as tethers to strengthen larger scale structures represents another class of applications. Quantum dots or zero-dimensional nanostructures are not suited for these applications. Quantum wells, or two-dimensional nanostructures may fit in well with some of the applications mentioned above; while in other cases, the design requirements are not met by these nanostructures either. Both 0D and 2D nanostructures, however, hold their own set of unique niche applications.

1.2.2 Current Challenges Facing Nanotechnology

Nanotechnology promises a bright future and a wide range of opportunities. However, in order to transfer nanoscale ideas from the laboratory into marketable products, a number of challenges must first be overcome. The areas of challenge fall into three main categories: nanoscale fabrication approach, assembly techniques and effects introduced at the nanoscale. This work addresses the fabrication approach and assembly techniques as one. Here, an integrated approach is developed.

1.2.2.1 Fabrication Approach

As we attempt to achieve smaller and smaller device dimensions, the transition from conventional IC fabrication processes (top-down) towards a regime similar to nature's ability to build up from smaller pieces (bottom-up) appears inevitable. Today's IC processes are physically limited to a minimum feature size and the costs associated with even minor improvements are extremely high. Therefore, it is

desirable to investigate the controllability of the bottom-up approach. The shift in approach, while economically favorable, places a large emphasis on the success of chemical/biological reactions thus introduces a new set of uncertainties and failure modes. More specifically, the ultimate goal is to understand these bottom-up methods such that the chemical/biological synthesis of nanostructures is well controlled yielding geometrically uniform, defect-free structures with a consistent set of electrical, mechanical and optical properties. Reliability and cost issues are at the core of this decision process.

1.2.2.2 Assembly Techniques

The discussion of assembly techniques really implies the need to develop robust, manufacturable and cost effective methods for the integration of the nanoscale with the outside world. As a microscale analogy, we may consider the wirebonding tool, a successful and highly dependable method of interfacing IC circuits, MEMS devices and other components with measurement and control tools, other components and ultimately the end user. The assembly process is as important as the nanostructure fabrication process. Well controlled nanostructure properties along with reliable and consistent assembly and interfacing methods are essential to realizing devices with uniform properties from device to device. Current nanoscale assembly and integration techniques are based on serial, expensive processes that are highly sensitive to environmental conditions, subject to low yield and display poor reproducibility. Therefore, massive, parallel assembly methods are being actively sought. The top-down/bottom-up choice comes up in this context as well and it is

now becoming clear that bottom-up methods cannot stand alone and that a successful approach would leverage elements of both bottom-up and top-down techniques. Therefore, another important issue that falls into this category is the compatibility of the bottom-up approach with other standard, commonly practiced top-down microfabrication processes and specifically thermal requirements and material compatibility issues.

1.2.2.3 Nanoscale Effects

Working on the nanoscale, at times, introduces phenomena not encountered on the micro and macro scales. These effects span two possible main thrusts, namely, (1) the general set of rules applicable to working on the nanoscale and (2) quantum effects which are normally only apparent on the extreme edge of the nanoscale, or the 1-10nm feature size. The former may address slightly altered electronic properties (limited mobility due to enhanced scattering, increased number of surface states) in 1-dimensional nanostructures when compared to their bulk counterparts while the latter addresses quantum confinement effects which may or may not be desirable. While this work wrestles with some of the issues that fall into the former category, the size scale and scope of the problem at hand do not fall into the realm of quantum effects.

2 Literature Review

2.1 Introduction

This chapter addresses the current state of nanoscale techniques and processes as they pertains to 1-dimensional nanostructure based fabrication, assembly, control and integration into functional devices. Specific emphasis is placed on the vapor-liquid-solid (VLS) nanowire growth mechanism as it is central to this work.

2.2 Background: Top-Down vs. Bottom-Up Approach

Top-down fabrication techniques or lithography based methods have traditionally served the IC industry as well as MEMS (micro-electromechanical systems) fabrication efforts. The top-down popularity stems from the ability to produce a wide range of shapes while providing consistent control over feature dimension from wafer to wafer. It is a parallel process with high throughput capabilities. Conventional lithography techniques, however, are limited by the minimum feature size possible. This limitation brings into question the role of top-down techniques in nanoscale fabrication. Modifications required to obtain nanoscale feature size have so far proved challenging and expensive [4].

Bottom-up fabrication techniques, on the other hand, involve building structures or molecules atom by atom; that is, beginning with the smallest component to realize

a larger assembly. This approach shares many of its attributes with biological processes and processes in nature. Since the process begins with the smallest of components, nanoscale resolution is easily obtained. Bottom-up processes are as a result of chemical and physical processes and hence share the randomness and reduced predictability associated with such reactions.

While the top-down approach for miniaturization of silicon is practical due to the extensive knowledge base associated with silicon processing, top-down fabrication of other nanomaterials is rather limited. Although both techniques offer a unique set of advantages and disadvantages, in this author's opinion a hybrid, integrated approach could be a most economical solution for miniaturization.

2.3 Nanoscale Fabrication Techniques: Chemical Synthesis of 1-Dimensional Nanostructures

2.3.1 The Vapor-Liquid-Solid (VLS) Growth Mechanism

The vapor-liquid-solid (VLS) growth mechanism has to date served as a workhorse for those in the nano community focusing on the bottom up synthesis of 1-dimensional nanostructures. This growth mechanism was initially developed in the 1960s to explain microscale whisker growth [5, 6]. These early studies focused on whisker cross sections ranging from ½μm to over 5μm wide. This growth phenomenon demonstrated a unique attribute, namely a significantly accelerated growth rate in the vertical direction when compared to the lateral growth rate. In other words, the VLS reaction produces high aspect ratio structures as the vertical growth is favored while lateral growth is essentially suppressed. The relevance of

this method to the nanoscale has recently been confirmed using direct in-situ transmission electron microscopy (TEM) observation [7], and the process can be used effectively to synthesize semiconducting and oxide based 1-dimensional nanostructures. While the requirements of the VLS process are rather well understood, the exact mechanism responsible for the reaction as well as the presence of physical limitations inherent to the process is still actively being studied.

2.3.1.1 General Attributes

The VLS mechanism requires the presence of a vapor phase and a liquid phase to realize a solid, 1-dimensional nanostructure while temperature is a significant enabler of this reaction, governing the initiation and continuation of the reaction. The vapor-phase precursor is the carrier of the desired nanowire material, where upon its thermal decomposition the desired nanowire material is available for the reaction. This reaction is different from a thin film deposition technique since in this case, molten metallic nanoparticles act as catalysts for the reaction by creating a preferred site for deposition. More specifically, the liquid surface is considered rough and capable of providing many more absorption sites, or a higher sticking coefficient (near 1) than do perfect or near perfect crystalline surfaces (<<1) [6, 8, 9]. The decomposed vapor-phase reactant is therefore preferentially deposited at these sites. Next, in order for the reaction to proceed, the metallic nanoparticle and the decomposed vapor phase reactant must form a liquid alloy at or above their eutectic temperature, as dictated by a binary phase diagram. The liquid alloy will continue to absorb the decomposed vapor phase reactants until the point of saturation is reached. Given a binary phase

diagram, the alloy will be located on the liquidus line at the specific synthesis temperature. Supersaturation will occur upon the additional deposition of the vapor phase reactant. Once supersaturation is reached the alloy will precipitate excess decomposed vapor-phase reactant in solid form and in an atom by atom fashion, yielding a single crystalline structure, which is dimensionally constrained by the cross section of the liquid alloy. This process is often referred to as tip growth process, as the precipitated solid is always found below the liquid alloy and, further, the presence of the metallic tip at the free end of the nanowire characterizes the VLS mechanism. Consequently, as a function of time, the 'newest' portion of the nanowire is always found just below the catalyst while the 'oldest' portion is found the furthest from it. As long as the vapor phase reactant and the corresponding thermal conditions are available, the supersaturation and precipitation process will continue, as incoming decomposed vapor-phase reactant replaces the precipitated portion. Also, there is little evidence that the metallic nanoparticle is consumed and nanowires 10s of microns long have been synthesized [10, 11]. Recent studies suggest that there is a minimum nanowire diameter which may be achieved using the VLS process, possibly limited size by the minimum stable size of the nanowire material crystal [12]. The VLS process is depicted schematically for silicon nanowire synthesis in Figure 2.1.

2.3.1.2 Silicon Nanowire Synthesis

For silicon nanowire synthesis the vapor phase reactant must yield silicon upon its thermal decomposition and the metallic nanoparticle catalyst must form a eutectic with silicon. Silane (SiH_4), disilane (Si_2H_6) and silicon tetrachloride ($SiCl_4$) are

commonly used vapor phase sources. The selection of an appropriate metallic catalyst is required to ensure that the VLS reaction will take place. A metal that is highly soluble in silicon, aluminum, for example, is not an effective catalyst as it will be consumed by the reaction. In other words, silicon must be soluble in the specific metallic catalyst and the precipitation reaction must yield the desired nanowire material rather than another compound [13]. Noble metals which are chemically inert are highly desirable for this process. Finally, the eutectic temperature of the metal-silicon alloy is important in the catalyst selection as lower temperature processes are more favorable in multi-step fabrication processes. A wide range of catalysts have been shown to effectively catalyze VLS based silicon nanowire synthesis, where a metal that forms a eutectic alloy with silicon is generally suitable for this reaction. While gold is the most commonly used catalyst, titanium, iron, nickel, gallium, zinc, and gold-palladium have also demonstrated to effectively catalyze the reaction [11, 14-21]. The various catalyst and vapor phase combinations yield a varying range of thermal requirements based on the catalyst-silicon alloy eutectic temperature, and the temperature required for the breakdown of the vapor phase. The low temperature gold-silicon eutectic (363ºC) and the low decomposition temperature of silane (~350ºC) enable a rather low temperature synthesis. In another example, although gold catalyst is used, the higher thermal decomposition temperature of $SiCl_4$, requires the reaction to be carried out at 800-850ºC [22], where the decomposition temperature is tied to the stability of the vapor-phase molecule [23]. On the other hand, using iron catalyst requires the reaction to take place at temperatures greater than 1150ºC due to

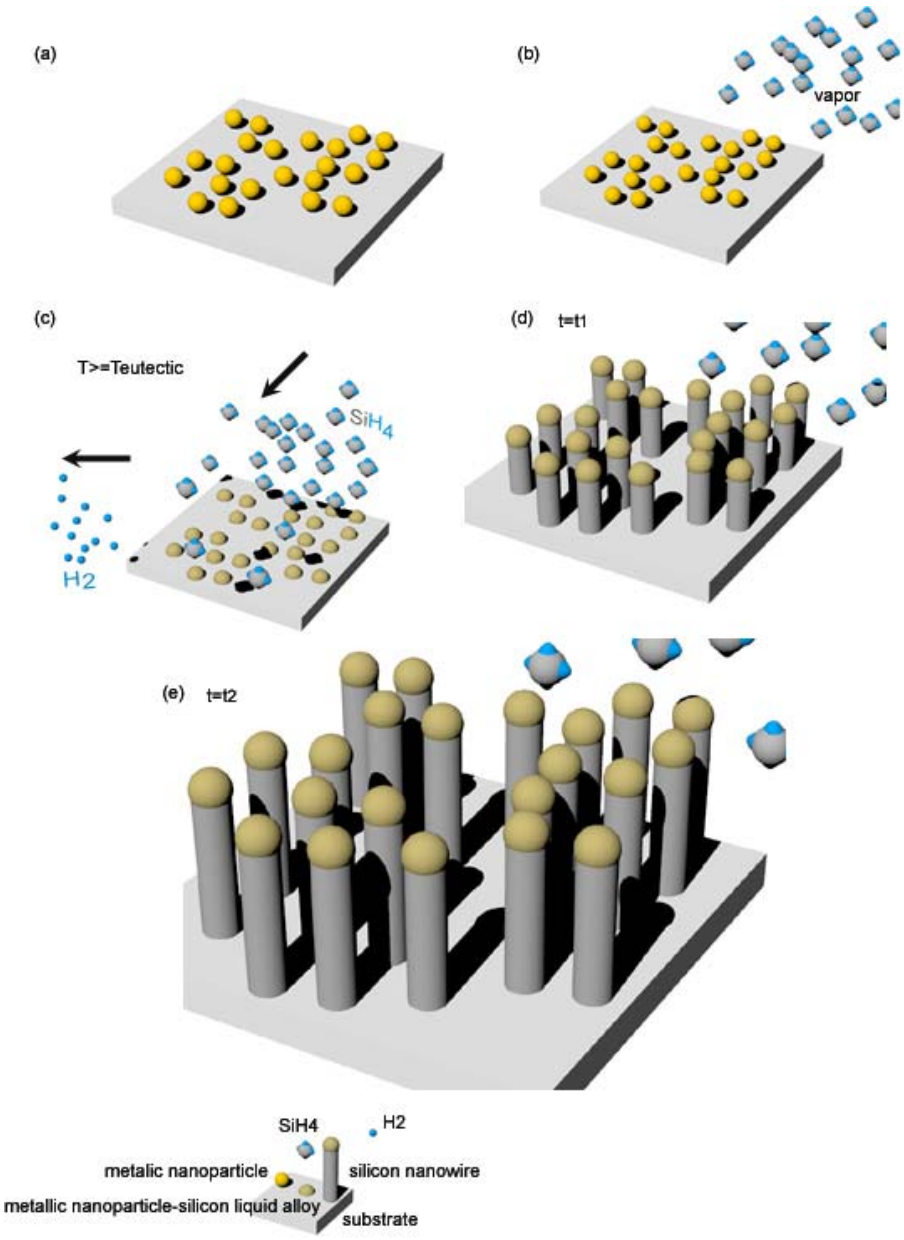

Figure 2.1. The VLS process for silicon nanowire synthesis. (a) Nanoscale metallic catalyst present on substrate. (b) Vapor phase (silane) reactant enters synthesis chamber. (c) Once the temperature requirements for the initiation of the VLS process are met, silane decomposes and preferentially deposits at catalyst location and a liquid alloy forms at the metal-silicon eutectic temperature. (d) Silicon continues to be absorbed by alloy until supersaturation is reached and silicon begins to precipitate from the alloy at the liquid solid interface, forming 1D nanowires. (e) Nanowire length is a function of growth time and growth conditions – reaction will continue as long as all elements are present (drawing not to scale).

the high temperature silicon-iron eutectic [17]. Table 2-1 presents operational VLS parameter combinations (pressure, flow rates and temperature) from the literature for gold-silicon (and gold-palladium-silicon) systems. Suitable VLS temperatures appear to range from 320-700ºC for the SiH_4 system and as expected are slightly higher for $SiCl_4$ based systems. The total chamber pressure is generally greater than 1Torr and may be significantly higher. The quality of the nanowires does vary with reaction parameters. More specifically, although a wide range of VLS process parameters have been shown to yield silicon nanowires, finding the unique combination of parameters that yields defect free nanowires is more challenging. Moreover, a systematic study of a wide range of pressure, flow rate, and temperature combinations, suitable for the VLS reaction, has yet to be conducted. In an early study [23, 24] utilizing a Au-SiH_4 system, a number of observations of the resulting nanowires as a function of the reaction's temperature and pressure were made. This study suggests that low pressures (0.1-0.5Torr) and moderate temperatures (480-600ºC) yield 'kink-free' silicon nanowires, while at low temperatures (<450ºC) and for all pressures greater than 2Torr, kinked nanowires result. This study further suggests a correlation between SiH_4 partial pressure and nanowire diameter as thinner nanowires result at increased synthesis pressure while lower pressures yield wider though less defective nanowires. Denser nanowire arrays and accelerated growth rates are also linked to increased pressure, and the increased growth rate is believed to be at least partially responsible to the increased kinking. In general, growth rates exhibited by silicon nanowires synthesized via the VLS mechanism are rather fast, especially when

Catalyst	Vapor Phase Reactant	Total Pressure (Torr)	$SiH_4/SiCl_4$ Flow Rate (sccm)	$SiH_4/SiCl_4$ Partial Pressure (Torr)	Synthesis Temperature (ºC)	Reference
Au	SiH_4	0.1-10	4	0.01-1	320-700	[23, 24]
Au	SiH_4	0.1	4	0.01	700	[25]
Au	SiH_4	----	15	----	500	[26]
Au	SiH_4	100	----	5	450	[27]
Au	SiH_4	100	15	5	450	[19]
Au	SiH_4	----	1-8	----	440	[10]
Au	SiH_4	5	----	----	450	[28]
Au	SiH_4	10	15	5	635	[29]
Au	SiH_4	100	3	50	435	[30]
Au	SiH_4	735	15	7.35	365-495	[12]
Au	$SiCl_4$	----	----	----	1050	[31]
Au	$SiCl_4$	----	----	----	800-850	[22]
AuPd	SiH_4	150	10	15	800	[20]
AuPd	SiH_4	0.350	10	0.035	550-700	[21]

Table 2-1. Functional pressure, flow rate and temperature combinations for the VLS reaction for Au-Si and AuPd-Si systems (dashed lines indicate that values were not reported).

compared to thin film growth, and a timed process can yield nanowires of a desired length. The growth rate as a function of temperature has been studied quantitatively in reference [12] and it has been demonstrated that over the temperature range of 365-495ºC, the growth rate increased from 0.012μm/min to 10.8μm/min.

In many cases the literature suggests that the diameter of VLS synthesized nanowires is slightly larger than the metallic nanoparticle that initiated the reaction, roughly following a linear relationship [10, 22, 30, 31] as seen in Figure 2.2 for a gold-silicon system independent of temperature and pressure. Evidence of the

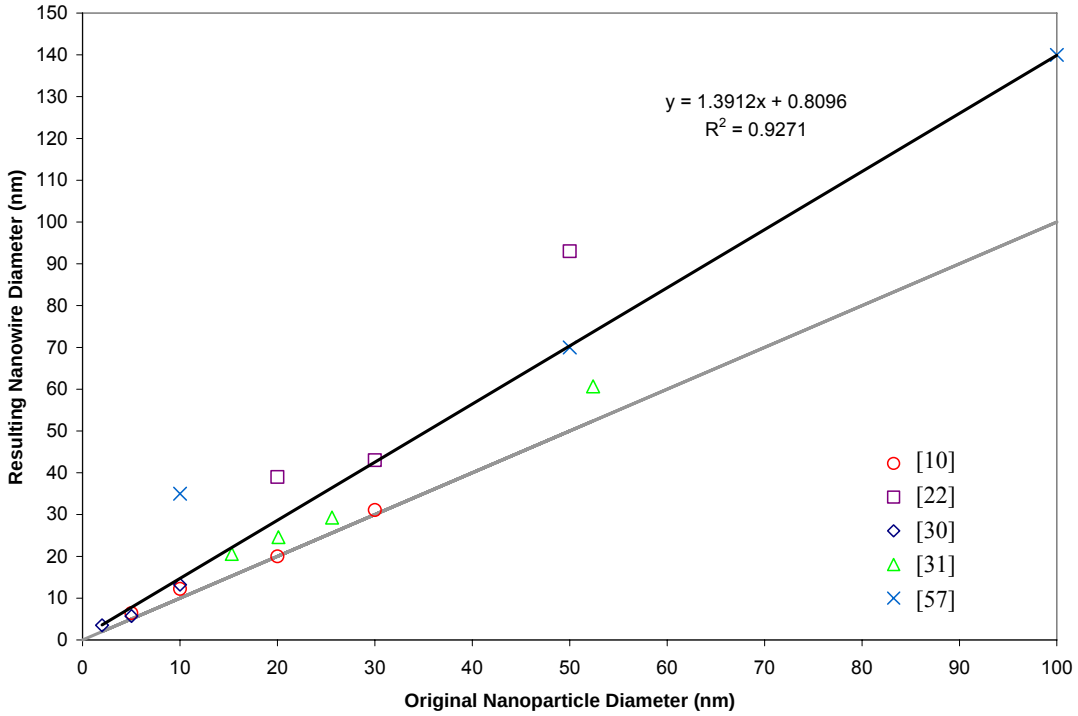

Figure 2.2. A correlation between initial nanoparticle catalyst diameter and resulting nanowire diameter based on data available in the literature. The relationship appears fairly linear (solid dark line) and the final nanowire diameter is always greater than the initial nanoparticle dimension. The gray line represents a 1:1 relationship between the two quantities.

opposite phenomena has also been documented but to a considerably lesser extent [28]. The former observation is expected as the initial catalyst increases in size upon the incorporation of silicon while the oxidation of silicon can also contribute a wider appearing nanowire [10]. It appears that the nanowire diameters presented in Figure 2.2 include the oxide layer as 2 of the 5 sources only acknowledge the presence of a very thin oxide while the other 3 do not mention accounting for the native oxide at all. As far as nanowire-final nanoparticle dimensional relationship and interface properties, TEM images often depict nanowires with a hemispherical catalyst at the tip, conforming to the nanowire diameter [10] as well as more spherical nanoparticles

slightly larger than the nanowires below [12]. Thermodynamic analysis suggests that the nanowire diameter should be somewhat smaller than the liquid alloy above it [9]. It is important to remember that initial catalyst size and the resulting nanoparticle at the tip of the nanowire at the end of the growth process may be different compositionally and dimensionally depending on the metal-silicon interaction and conditions at termination of synthesis process. Silicon nanowires as small as 3nm in diameter [30] have been successfully synthesized, and it appears that the minimum silicon nanowire diameter achievable using the VLS method is approximately 1nm [12].

Finally, VLS synthesized silicon nanowires often tend to grow along the <111> direction presumably because it is the lowest energy plane. More specifically, it is believed that the <111> direction is favored as it provides the lowest liquid-solid interfacial energy [30, 32]. More recent observations also suggest that smaller diameter nanowires (≤ 20nm) exhibit the <110> and <112> directions as the preferred growth directions, where these cases are most likely mediated by the surface energy of the silicon nanowire. Interestingly, the non <111> growth orientation introduces a different silicon-catalyst interface, no longer producing a flat interface [30].

2.3.1.3 The VLS Mechanism & Nanoscale Doping

Bulk and thin film doping of silicon as well as other semiconductors is a relatively standard process. Ion implantation techniques as well as the introduction of dopants into the flow stream, in a furnace environment, are commonly practiced methods. As the literature suggests, the introduction of a dopant source into the

nanowire synthesis environment is a suitable approach for achieving reasonable doping levels and does not adversely affect the VLS process. Developing controlled and consistent nanoscale doping scheme is crucial to realizing the full potential of 1-dimensional semiconducting nanostructures.

Reliable p-type doping of silicon nanowires was demonstrated by adding either the traditionally utilized diborane (B_2H_6) [33] or the organometal precursor trimethylboron ($(CH_3)_3B$, or TMB) [34] to the flow stream. The doping level is controlled by the silane to dopant gas flow ratio. While reference [33] examines silicon nanowire properties in two distinct cases (SiH_4:B_2H_6 –1000:1 & 2:1), and reference [34] examines a range of doping levels, 25,000:1 to 62.5:1 (SiH_4:TMB), much of the follow up work and device applications have been successfully conducted using a 4000:1 (SiH_4:dopant) ratio [35, 36]. N-type nanowire doping using a phosphine (PH_3) source in combination with silane was recently described [37], and again the SiH_4:PH_3 ratios range from 4000:1 to 500:1. TEM analysis of the doped nanowires suggests that the single crystalline nature of the nanowires is maintained while I-V characterization establishes the success of the doping process. Although doped nanowires do exhibit improved electrical properties when compared to their intrinsic counterparts, mobilities [33] and resistances [34] fail to match bulk values associated with specific doping levels. It is hypothesized that either the enhanced scattering in the nanostructure, the quality of the contacts, or both may influence the measurements. In fact, refinements of electron beam lithography techniques over the last few years could potentially improve the results presented in reference [33]. The

reported nanowire diameters doped in this fashion range from 20-90nm. It appears, however, that nanoscale doping it not completely understood and still poses a challenge, especially in smaller diameter nanowires. Concerns include the "closer proximity of the surface" which make the diffusion length to surface short and thus suggests that a dopant atom does not have to travel very far before it is no longer electrically active [38].

2.3.2 Oxide Assisted Growth of 1-Dimensional Nanostructures

Another popular bottom-up, chemical nanowire synthesis method is known as the oxide assisted growth (OAG) method. The most significant difference between OAG and the VLS mechanism is that a metallic catalyst is not required for the OAG to take place; instead, an oxide plays a significant role [39, 40]. More importantly, the resulting nanowires are pure and metal free. The synthesis process is initiated by laser ablation of silicon and silicon dioxide powers, for example, in a high temperature environment to yield silicon nanowire growth. The amount of oxide present in the original target is directly related to the amount and growth rate of the silicon nanowires produced. It is believed that the presence of defects may mediate this growth process. Further it appears that a silicon oxide seed develops and becomes enveloped by an oxide layer which forms as oxygen is expelled from the seed by the growing silicon nanowire. The oxide layer is believed to constrain horizontal growth, while a semi-liquid, reactive oxide at the tip, acts as a sink for incoming species and the growth process proceeds as silicon-silicon bonds preferentially form from silicon oxide clusters [39]. Nanowire diameters approaching

1nm have been reported, however, diameter distribution and nanowire uniformity appear more difficult to control when compared to the VLS process [39, 41].

2.4 Organization, Assembly and Integration of Nanostructures

As previously discussed, establishing controlled methods for 1-dimensional nanostructures synthesis is only a part of the requirements for developing nanoscale systems and devices. Techniques for directing 1-dimensional nanostructure growth and improving nanostructure organization are directly tied to the ultimate goal of establishing manufacturable nanostructure-based systems and devices. Such techniques are particularly favorable if a parallel process can be devised so that the manipulation of multiple nanostructures simultaneously is possible.

2.4.1 Electric-Field Based Methods

Electric-field based methods are attractive due to the simple setup required and minimal interaction with the nanostructures. In order to take advantage of the electric-field effect all that is required is maintaining a voltage drop over a specific region occupied by nanostructures.

Previously, 1-dimensional nanostructures such as carbon nanotubes (CNT) have been shown to respond to the presence of a DC electric field during synthesis to yield a better organized growth pattern as nanotubes follow electric field lines [42-44]. This behavior is attributed to the strong polarizability of these 1-dimensional nanostructures [45] and the electrophoretic effect. More specifically, the interaction mechanism is based on torque created on a CNT polarized by the electric-field which

results in CNT growth along electric field lines. The torque is shown to be directly proportional to the applied electric field strength squared [42, 43]. This approach permits the alignment of CNT during their synthesis process.

The post-synthesis control and placement of CNT, metallic and doped semiconducting nanowires using DC, AC and composite electric fields, in solution (typically ethanol), has been widely demonstrated [46-51]. In these experiments both ends of the nanostructure are free to interact with the field and dielectrophoretic interactions play a significant role. The CNT response to purely DC fields, in these cases, is reported to be rather minimal [48-50]. This process, however, is not compatible with in-situ-growth alignment needs and is limited due to the strong dependence on the evaporation time of the liquid solution.

It is reasonable to conclude that a conductive one-dimensional nanostructure is required to realize a response to an electric field, and as such these methods are not compatible with insulators, for example. The in-situ response of semiconducting CNT, however, has been documented for CNT over a minimum length [42, 52]. Reference [42] further suggest that although the polarizability of metallic CNT is approximately 3 times greater than that of a semiconducting CNT, if the CNT's energy of rotation, introduced by the electric-field induced torque, is greater than its thermal excitation energy (kT), a response to the presence of an electric-field is possible. The energy of rotation is shown to be proportional to CNT's length [42]. Hence, longer nanostructures are expected to show a more significant effect.

2.4.2 Fluidic Based Methods

Fluidic based methods have been shown to assist in aligning multiple nanostructures along the direction of flow in microfluidic channels. The alignment mechanism is attributed to a shear flow regime at the bottom of the microfluidic channel [53, 54]. It appears that better alignment is achieved with higher flow rates as more significant shear forces are developed. This technique was further extended to build more complex, layered, crossed systems of nanostructures by simply changing the direction of flow with each layer. The surface properties of the channel also play a significant role in the alignment results. Timing is critical in this process, as the nanostructures eventually become immobilized on the surface and as such process parameters (surface treatment, environmental conditions) must be carefully controlled to permit alignment prior to immobilization. Surface treatments, chemical activation and pre-patterning of the channel surface have contributed to improved results, however, at the cost of increasing the tediousness of the technique [54].

In an improvement over the basic microfluidic flow approach, the concept of Langmuir-Blodgett technique has been shown to enable massively parallel 1-dimensional nanostructure alignment in a fluid environment [55, 56]. Here, a single layer of nanowires is resting on the water surface in a Langmuir-Blodgett trough and as a result of the compression of the trough's opening the nanowires align parallel to the trough's borders. The trough's compression determines nanowire spacing. At full compression, a closed packed, single layer of nanowires is obtained. Crossed, complex systems can be built by stacking multiple compressed layers [55, 56].

2.4.3 Electron Beam Lithography Based Integration & Assembly

It is not only important to efficiently and controllably synthesize and place 1-dimensional nanostructures, but further, in order to make these functional, the nanostructures must be able to communicate with the outside world.

Electron Beam Lithography (EBL) is an indispensable tool as it is essentially a mask-less lithography process permitting fine (<100nm) feature writing and arbitrary geometry capabilities inside a scanning electron microscope (SEM). EBL is also commonly used for making high resolution masks for typical photolithography applications. Focusing an electron beam onto an electron-beam sensitive resist surface to expose a specific location is the core principle behind EBL operation.

As far as nanoscale device fabrication, EBL is the tool commonly utilized to generate mechanical and electrical contacts [1]. Typically the desired nanostructures would be synthesized using a bottom-up technique. If the nanostructures are synthesized in contact with a substrate, a sonication step is required to remove the nanostructures from the surface. Next, the nanostructures are placed in solution and dispensed, in small volumes, onto a desired device substrate. Van der Waals forces ensure that the nanostructures adhere to the substrate. The device substrate usually includes a dielectric surface and pre-patterned metallic electrodes which serve as contact locations. This substrate surface is then coated with an electron-sensitive resist. Next, 'suitable' nanostructures are located on the prepared surface using a SEM. Ideally, unbent nanostructures with no or minimal interaction with neighboring nanostructures, in relatively close proximity to and the correct orientation with

respect to the predefined electrodes are sought. The EBL step follows, and requires defining a contact to the desired nanostructure and a contact path to a nearby electrode. For a typical 1-dimensional nanostructure based device, the EBL process is performed at each end. The EBL process sets up a lift-off metallization process and a metal layer is evaporated next. Generally, a thermal evaporation process is used so that sample is exposed to a minimal surface temperature change. Finally, the resist layer is etched and removed and the device is complete. More complex devices may require additional processing and contact formation. When properly executed this approach ensures reliable contacts, however, the deterioration of the contacts with time has been suggested as a possible disadvantage [57].

2.5 Demonstration of Silicon Nanowire Based Applications

The allure of the nanoscale is its being an enabler for better, faster and cheaper devices and systems. The literature offers a wide range of prototypes illustrating various applications, yet the most mature silicon nanowire based applications come from the Lieber Group at Harvard University. The success of this group is largely due to their ability to carefully and consistently control the electrical properties of VLS synthesized silicon nanowires. Silicon nanowire based sensing applications have been studied in depth and the sensing mechanism exploited in their work is a direct electrical sensing approach utilizing nanowire based field effect transistors (FETs) [2]. More specifically, a doped nanowire serves as the gate electrode of the FET. The binding of specific species to the surface leads either the accumulation or depletion of carriers and hence a recordable change in conductance. The nanowire

surface must be modified to enable specific detection needs. Using this approach, solution based pH sensing as well as specific DNA, protein and virus detection was demonstrated [35, 58]. The high sensitivity of these devices and well as the real time operation and minimal species requirements make this approach extremely attractive. Silicon nanowire based nanoelectronics have also been demonstrated in the form of diodes, FETs and logic gates configurations [54]. Doped silicon nanowire based FETs appear to be extremely versatile and have shown equivalent or improved device characteristics when compared to devices produced by the microelectronics industry [2, 37]. Although the reproducibility of these devices has been demonstrated, the fabrication process relies heavily upon serial EBL based processes for contact definition, assembly and integration.

3 Localized Synthesis of Silicon Nanowires

3.1 Introduction

At the center of this work is the ability to finely control the extent of silicon nanowire growth by enabling the VLS reaction to take place only at a select region determined by meeting the VLS reaction's thermal requirements. While many have accurately controlled the location of the catalyst and hence achieved selective growth patterns, never before has the thermal requirement of the VLS reaction been spatially controlled. The ability to confine the heating to specific regions on a chip, for example, rather than subjecting the chip to a global heating environment, opens up a wide range of opportunities for nanotechnology. The role of this process in the direct integration of nanostructures with larger scale systems, while offering a CMOS compatible option and the flexibility of adding nanostructures as the final step in the fabrication process introduce significant advantages over traditional methods.

3.2 Localized Synthesis via Localized Heating

3.2.1 Design Consideration for the Microscale Platform

Achieving localized synthesis requires a method for initiating and sustaining the required heating locally, at confined regions. Simple silicon based MEMS structures, such as narrow silicon beams or essentially wires [59-61] have been shown to mimic

resistor behavior and reach a wide range of temperatures upon the application of power across their terminals through the concept of Joule heating. With these beams, it is possible to control the level of heating by controlling the input power, and the applicable temperature range covers room-temperature through the melting temperature of silicon (1440ºC). Moreover, these silicon beams have been shown to function as incandescent light sources, and glow brightly when electrically heated [62]. Hence it is possible to correlate the power input with the optical response to roughly gauge surface temperature. Utilizing structures of this general configuration is advantageous as they are simple to design and may be fabricated using standard microfabrication processes while enabling a location confined heating regime and thus meeting the requirements of the CMOS compatible localized synthesis process.

Design considerations for such resistive heaters were developed based on the requirements of the VLS process and the need to truly achieve a localized heating regime. More specifically, the requirements include geometrical attributes and material resistivity that permit heating in the 500-1000ºC temperature range while minimizing physical damage to the structure, confining the extent of the heating to the structure itself and reducing the power required to achieve the desired heating level. In addition, these structures must be electrically and thermally isolated from the substrate and able to relieve thermal stresses without altering the temperature distribution. Electrical isolation is necessary to eliminate a possible short to the substrate by virtue of the catalyst required for the VLS process as well as to eliminate cross-talk through the chip which may interfere with electrical characterization.

Thermal isolation from the substrate is important as it enables heating at reasonable power consumption, eliminates conductive heat dissipation to the substrate and as such ensures that all regions of the chip, but the heated structure, remain at room temperature.

Ideally, a simple suspended fixed-fixed beam should be able to satisfactorily meet the design constraints. The only limitation to this design is that a straight, fixed-fixed beam design may only relieve induced stresses by moving vertically out of plane. This limitation serves to alter the heating profile through the heater as seen in Figure 3.1. The Figure illustrates an optical microscope image (in light and dark) of a resistively heated fixed-fixed beam. While the center of the beam appears dark, two off-center locations are hot and brightly glowing. The dark region is due to the beam buckling towards the substrate and as such increasing the heat dissipation rate and reducing the temperature at the central region. The light image clearly shows the center of the structure approaching the substrate.

The limitations of the straight beam design were mitigated by utilizing suspended U-shaped MEMS structures, comprising of three sections, as illustrated in Figure 3.2. The U-shaped MEMS structures were found to adequately meet design requirements as this design features unconstrained corners permitting lateral motion of the structure and thus enabling in-plane accommodation of induced stresses and thermal expansion. This design was therefore selected to function as the preferred nanowire synthesis platform, and the dimensions of these structures are discussed in conjunction with the fabrication process.

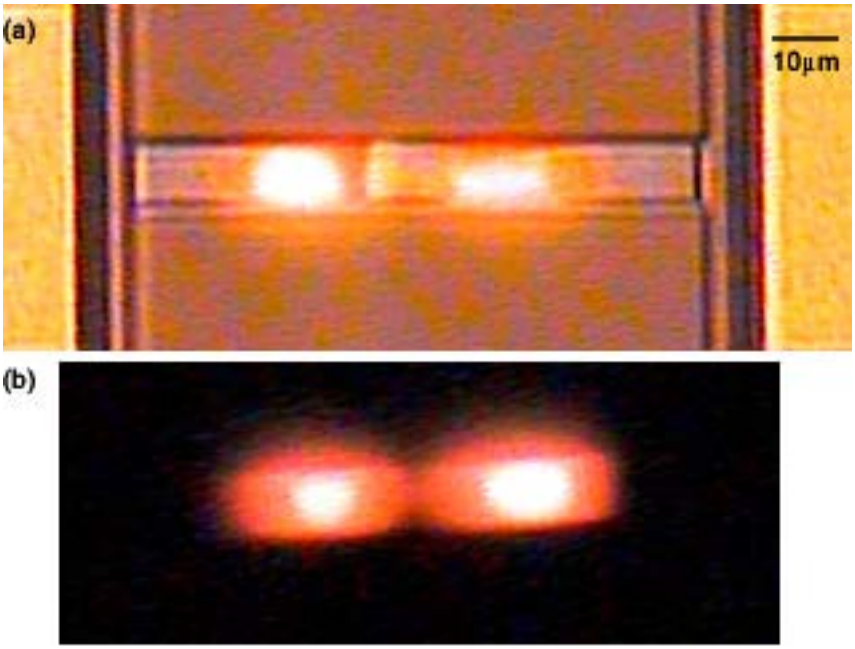

Figure 3.1. An optical microscope (light and dark) image of a straight 100μm long and 10μm wide MEMS polysilicon structure subject to Joule heating. The glowing regions correspond to high temperature regions. In (a) the buckling of the structure towards the substrate is clearly seen, and in (b) the dark image confirms a low temperature region in the center as the glowing is significantly minimized.

3.2.2 MEMS Platform Fabrication

Inline with the overall goal of developing a CMOS compatible process, the MEMS structures' fabrication process followed standard, well characterized microfabrication techniques. Along these lines, silicon was the MEMS structure material of choice. More specifically, both single-crystal silicon (SCS) and polycrystalline silicon MEMS structures were explored as synthesis surfaces, although other conductors and semiconductors compatible with micromachining technologies and capable of sustaining the localized temperature through the duration of the synthesis process could ideally be used, as the surface does not actively

participate in the VLS reaction. Since the preferred growth orientation for silicon nanowires is the <111> direction, a <111> oriented synthesis surface does offer the ability to better control the nanowire's growth orientation as nanowires grow perpendicular to the synthesis surface [22, 31]; however, this aspect was not actively pursued in this work.

The SCS MEMS structures were fabricated using silicon on insulator (SOI) wafers via bulk micromachining technology [63] while the polysilicon MEMS structures were fabricated using surface micromachining processes [64] offered by the MUMPs™ foundry process. SOI wafers offer a highly and uniformly doped device layers, important for reliable MEMS structure actuation and heating as well as a thick silicon dioxide layer, important for electric and thermal insulation from the substrate. In addition, these wafers require only a single lithography step to realize the desired MEMS structures. The lithography step is followed by the deep reactive ion etch (DRIE) step etching the silicon device layer where desired (Figure 3.2). On the other hand, the MUMPs™ process offers additional flexibility with multiple structural layers and a metallization layer. The MEMS structures were fabricated from both, heavily doped p-type and n-type SOI wafers, while the MUMPs™ foundry process produces heavily doped n-type polysilicon structural layers. Appendix 9.1 lists the properties of the synthesis platforms used in this work. The low resistivity resulted in low resistance MEMS structures that could be heated to the required synthesis temperature with ≤ 10Volts applied and low power input of ≤ 0.4Watts. The dimensions of the MEMS structures were chosen to comply with the low

resistance requirements while meeting lithography dependent design rules and yielding mechanically robust structures. Tests indicated that thinner structures show more damage as a result of the heating process than do thicker structures and therefore SOI wafers with thick device layers (15-50μm) and thick MUMPs™ structural layers (poly 2-3.5μm thick) were the favorable synthesis platforms. The width of the MEMS structures was minimized to further confine the synthesis region and was generally designed to be 5μm wide. Shorter structures were desirable for both structural integrity and resistance reduction purposes as resistance is directly proportional to length. Typically, the U-shaped structures were designed to have two 50μm long segments and a central segment measuring either 50μm or 100μm long. The thickness of the oxide layer of the SOI wafers (1-2μm) and the thickness of the first sacrificial oxide layer in the MUMPs™ process (2μm) were used to define the distance between the MEMS structure and the substrate. As mandated by the design constraints, this gap is necessary for electrical and thermal isolation. Once fabricated, the structures were released in a timed wet oxide etch in 49% hydrofluoric (HF) acid to produce suspended MEMS structures, and a hydrogen terminated silicon surface. The etch time was governed by the widest feature to be released and due to the narrow structure design was relatively fast at 2-2.5 minutes. A final consideration with respect to the MEMS structure design is anchor design, where the anchors are designed to be significantly larger than the MEMS structures' beams to ensure good mechanical contact to the substrate after the wet release process. Typical anchor dimensions are 200μm by 200μm. Large anchors are also essential for actuation and

characterization efforts as will be discussed in the following chapters. The fabrication process yields multiple chips with variety of MEMS platforms for silicon nanowire synthesis.

3.2.3 Experimental Setup

The fabricated MEMS structures were then prepared for the VLS process. The only requirement is the placement of the metallic catalyst onto the reaction surface. The catalyst selection is an important parameter defining the temperature requirements of the reaction. Metals forming a high temperature eutectic with silicon were not considered and instead a gold-palladium mixture was selected. While in many cases the catalyst's location is spatially controlled to confine the extent of the VLS reaction, since here localized heating is used to activate the VLS reaction, a thin layer of catalyst was deposited chip-wide without the need for an additional catalyst patterning step. More specifically, a sputtering tool manufactured by the Technics Corporation was used to deposit approximately 5nm of a gold-palladium ($Au_{0.6}Pd_{0.4}$) mixture at room temperature and 200mTorr. The deposition time lasted 30 seconds and the thin film thickness was confirmed by using AFM step height measurements. Since the catalyst layer is thin and due to the wet release process that naturally creates recessed regions beneath the anchors, there are no concerns about the mask-less catalyst deposition process contributing to an electrical short-circuit.

Next, an individual chip was attached to a chip carrier and individual MEMS structures were wirebonded to create electrical contacts to the structure. A semi-packaged chip results prior to the nanowire synthesis process, indicating that the

synthesis step could indeed be the last fabrication step. In order to improve productivity of the synthesis process 5 to 10 synthesis platforms were wirebonded for each run.

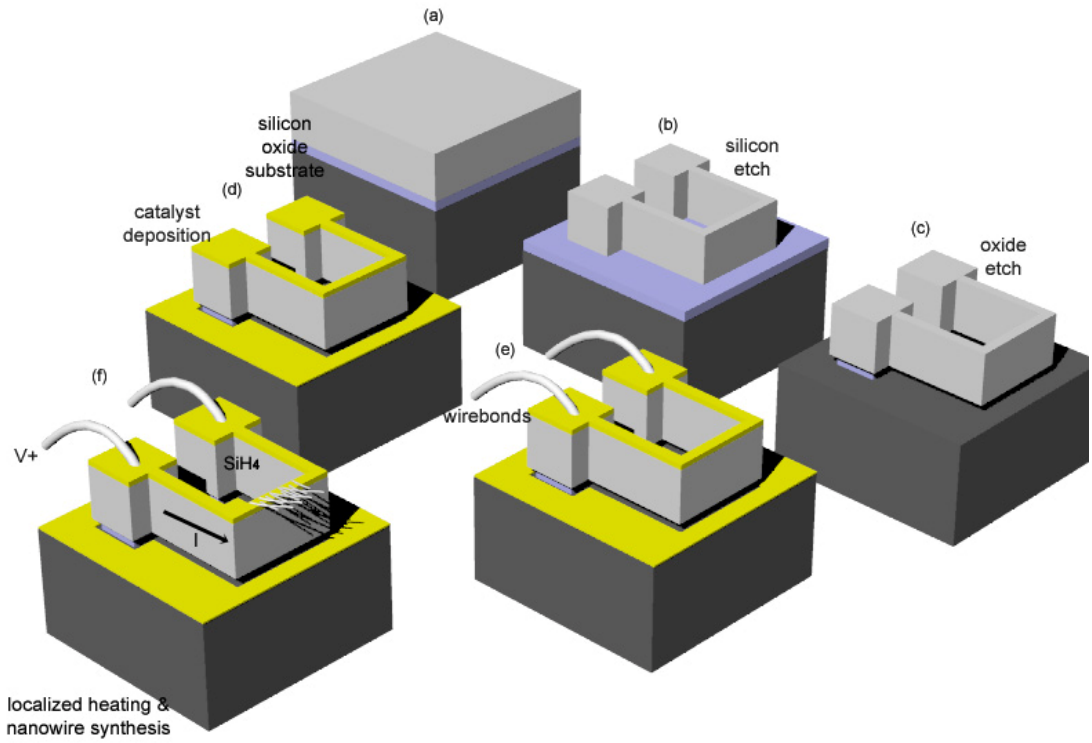

Figure 3.2. MEMS structure fabrication, preparation for localized VLS and localized VLS experimental sequence. (a) Starting SOI wafer. (b) Definition of MEMS structures and silicon etch. (c) Wet oxide isotropic etch step to realize suspended structures. (d) Mask-less catalyst deposition. (e) Wirebonding individual structures. (f) Localized heating in presence of the vapor phase reactant to yield silicon nanowire synthesis.

The VLS reaction takes place inside a room temperature vacuum chamber. The vacuum chamber used for the purpose of this experiment, manufactured by Technics Corporation, was originally designed to serve as a PECVD (plasma enhanced chemical vapor deposition) tool, and was converted for this purpose. The plasma functionality of the PECVD tool was never utilized, as the thermal decomposition of

the vapor phase reactant was sought. Since the heating element was not needed, as the localized heating scheme is employed, the heater platen was removed and the thermocouple's wiring opening consequently created the ideal location for the wiring feedthrough required to enable remote communication with individual MEMS structures. Although a very basic component, the feedthrough was critical to enabling this process. It is a hollow aluminum tube with an outer diameter measuring a half inch designed to match the chamber's wiring opening. Copper wires extend through the tube and the tube is filled with dense epoxy to create a good seal to maintain vacuum and prevent leakage through the tube. Ensuring a leak proof interface is crucial due to the toxicity and flammability of the gases used in this process and as such multiple safety checks were performed. Once the chamber was prepared, the semi-packaged chip, attached to a plastic breadboard, was placed inside the vacuum chamber. Using the feedthrough's wires the MEMS structures were connected to a power supply for remote actuation and to a pair of multimeters for feedback and control. The experimental setup is illustrated in Figure 3.3.

The synthesis process begins by evacuating the chamber to a baseline pressure (typically 30-40mTorr). Next, the VLS process is initiated by introducing the vapor phase reactant, 100sccm silane (10% SiH_4/ balance Ar). In the absence of direct control over the total chamber pressure, the chamber pressure was controlled by SiH_4/Ar flow rate. Over the range of experiments performed in this work, during a three year period, the chamber pressure varied from 190mTorr to 400mTorr where the SiH_4/Ar flow rate is fixed at 100sccm. The partial pressure of SiH_4 is always 10%

Figure 3.3. Experimental setup. (a) Overview of synthesis chamber and auxiliary control & feedback electronics for localized heating. The blue arrows mark the path to the sample. The unit's flow controller is at the bottom right. (b) A side view of the synthesis chamber showing the external connection to the feedthrough (chamber is closed). (c) A view of the feedthrough connecting the inside of the chamber (top) to the outside (bottom) and the electrically connected sample resting inside the synthesis chamber (d).

of the total chamber pressure. The variation in chamber pressure was due to changes and upgrades to the flow lines of the unit. The change in pressure appears to be related to the growth rate and will be discussed in more detail in the results section.

With silane flowing in the chamber, the localized heating process is initiated by applying a voltage across the terminals of an individual MEMS structure. The specifics of this process are discussed in the next section. Once the desired heating level is reached, the experimental parameters are held constant. It was confirmed that MEMS structures used in these experiments could sustain the localized heating and the extent of the hot spot, or glowing region, under constant voltage for long periods of time. Optical microscope tests lasting up to an hour long confirmed this characteristic of the MEMS structures. Finally, since the length of the synthesized nanowires is a function of growth time, the reaction time was adjusted to achieve the desired nanowire length.

3.2.4 Thermal Considerations

The surface temperature of the MEMS structures must meet the temperature required to initiate and sustain the VLS process. The temperature of the MEMS structure is assessed based on the geometry, doping level, and current-voltage characteristics [60]. Typically, the current-voltage curve is characteristically linear under low input power and becomes non-linear when the input power is high as seen in Figure 3.4. More specifically, at low temperatures a linear I-V relationship is expected for these MEMS structures as these structures behave essentially as resistors. However, at increased voltage and as such increased power generation and elevated

temperatures, the linear relationship terminates and, instead, the curve flattens. This behavior is consistent with theory as the increased scattering caused lattice vibration at elevated temperatures limit the mobility of charged carriers in doped semiconductors [65].

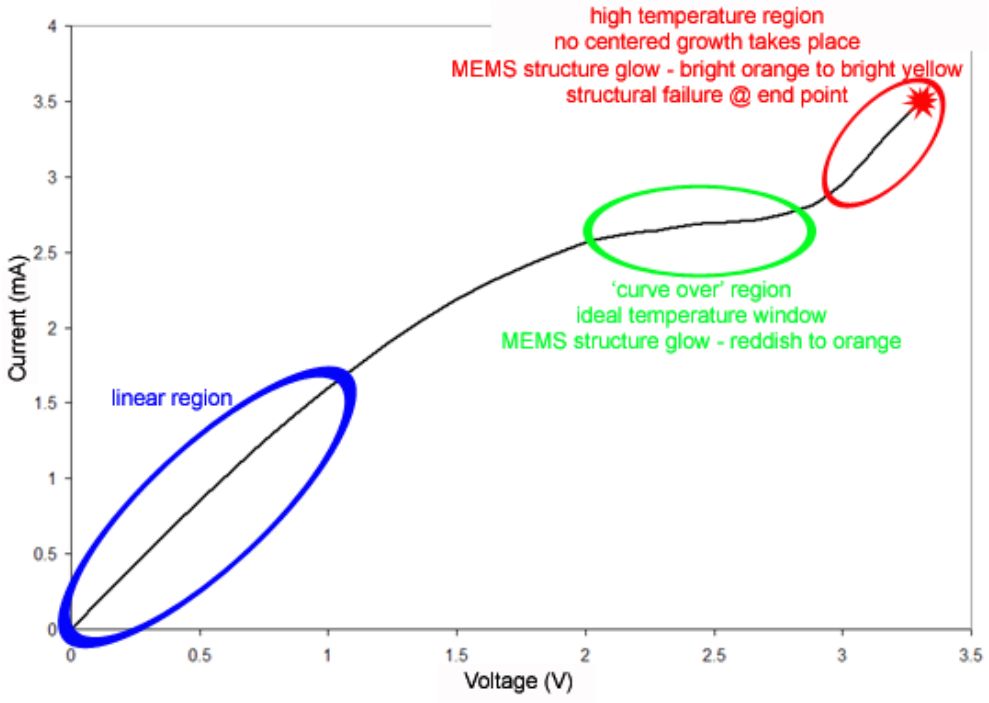

Figure 3.4. I-V curve representing the resistive heating of a typical MEMS structure. The structure initially behaves as a resistor (linear region). Upon additional power input, the 'curve over' region is reached entering the ideal temperature region for silicon nanowire synthesis and producing associated glowing. Finally, the high temperature region is entered eventually leading to the failure of the structure.

It is possible to correlate the optical response of these structures with a location along their I-V curve. Using an optical microscope, the color and intensity of the surface of the MEMS structures as a function of applied voltage can be observed, as illustrated in Figure 3.1, for example. Visually, a reddish glow appears to correspond

to the 'curve over', or zero slope region of the I-V curve and designates the approximate temperature range required for the VLS process in this AuPd-Si system to take place. The MEMS structure's glow, however, could not be observed during the actual synthesis process, as the vacuum chamber is not accessible to an optical microscope. The required temperature range was therefore associated with the 'curve over' behavior of the I-V curve and thus provided an estimate of the required voltage input to the MEMS structure. This association was critical in assessing that the required synthesis temperature range was achieved since the experimental setup creates a 'blind' process as the operator cannot visually assess the level of heating in the MEMS structure. Therefore, by applying and steadily incrementing the voltage while observing the change in current until the current-curve-over region is reached, localized resistive heating of the suspended MEMS structure can be monitored. While a certain minimum temperature must be reached for the VLS reaction to take place, maintaining the temperature below failure point, or the melting point of silicon is equally important. It is important to mention that the I-V characteristics of each set of MEMS structures was slightly different primarily based on active layer type, doping level, and to some extent the dopant type. Further, within each set, the I-V characteristics varied with structure length. Each set of MEMS structures was characterized prior to the synthesis process.

FEMLAB® software was used to develop a finite element model to determine the temperature profile through the resistively heated MEMS structure. The model predicts a parabolic temperature distribution through the MEMS structure where the

hottest location is at the center of the structure while the anchors remain at room temperature. The steady state model follows a two step analysis; an electrostatic analysis accounting for potential difference through the MEMS structure, followed by a heat transfer analysis evaluating temperature profile due to the resulting heat generation. The energy balance and heat generation term are expressed in Equations 3-1 and 3-2, where k is the thermal conductivity, T is the temperature, q''' is the volumetric heat generation term, J is the current density, σ is the conductivity, and E is the electric-field. While secondary effects contribute to the volumetric heat

$$\nabla \cdot (k \nabla T) = -q''' \qquad \text{Equation 3-1}$$

$$q''' = \frac{J^2}{\sigma} = JE = \frac{IV}{volume} \qquad \text{Equation 3-2}$$

generation term, the resistive heating component is the dominant term and solely used for simulation purposes. Radiation effects along with the heat generation due to recombination of holes and electrons may be neglected as they are considered negligible [66]. Furthermore, the low pressure synthesis environment virtually eliminates any convection heat losses and the suspended structure is treated as thermally insulated. Therefore, the most significant heat loss takes place at the anchors via solid state conduction as the anchors are set at room temperature as a boundary condition. The conductivity of silicon as a function of temperature and the mobility decrease in doped silicon at high temperatures are accounted for in the model [65, 67]. A typical model result is seen in Figure 3.5. The model's results are in agreement with experimental actuation parameters and the temperature profile is

consistent with optical observations (i.e. glowing region at the center which fades towards the ends). When a potential difference value greater than typical experimental actuation parameters is applied in the model (i.e., 8V inputted into model while 6V were necessary to sufficiently heat the structure during the experiment), the model's output suggests a peak MEMS structure temperature higher

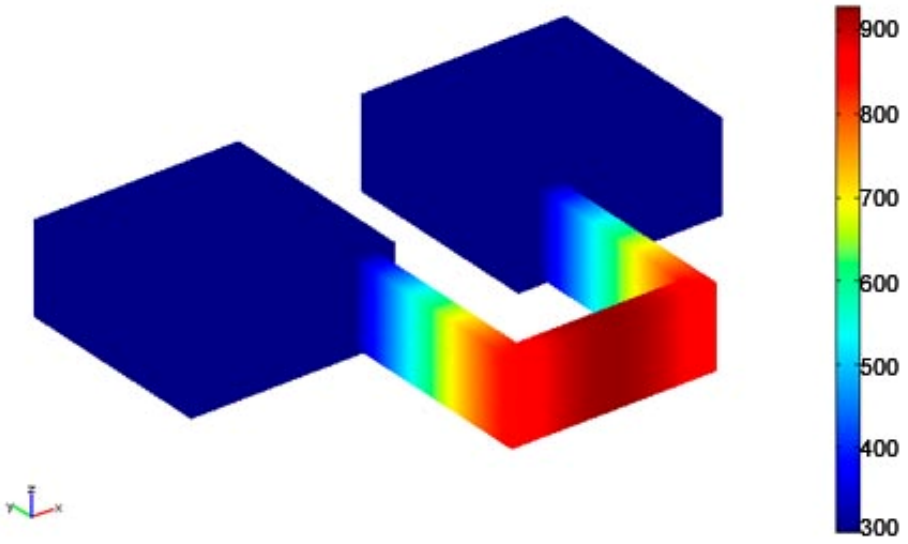

Figure 3.5. Electro thermal modeling results for a 150μm long, 5μm wide and 20μm thick MEMS structure (the temperature scale is in degree K). The maximum temperature at the center is 930K (657ºC), and the hottest region spans approximately 20μm.

than the melting temperature of silicon indicating that such input values are not reasonable for this process, and further increasing confidence in the model. Figure 3.6 illustrates the simulated temperature distribution as well as the relationship between the maximum temperature and the applied voltage as predicted by the model for a typical MEMS structure. The results also indicate that an input difference of as little as a tenth of a volt is equivalent to an 8 to 10 degree shift in the maximum temperature. This fact illustrates importance of pinpointing the appropriate I-V input

required for the VLS process to take place and truly exemplifies the trickiest aspect of this process. Further, the model confirms that as the maximum temperature of the MEMS structure increases, more significant temperature gradients are present through the structure since the thermal boundary conditions must be met. This behavior relates to the extent of the nanowire synthesis region as will be addressed in the results section.

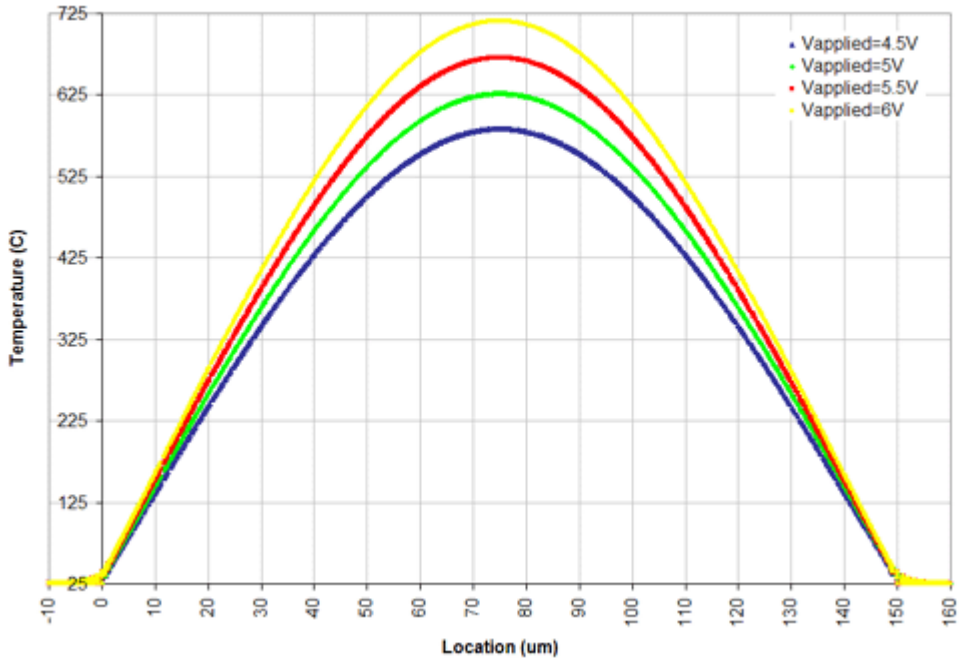

Figure 3.6. Temperature distribution through a 150μm-long MEMS structure when subject to various applied voltages. (Only a limited portion of the room temperature anchors is displayed). As the input voltage is increased so does the maximum temperature. An input difference of ½V may correspond to a 40ºC difference in temperature thus illustrating the importance of identifying the necessary input to meet the temperature requirements of the VLS process. Temperature gradients associated with the resistive heating process may also be evaluated from the plot.

As previously discussed, the VLS reaction proceeds as a number of sequential temperature dependent processes take place [24]. First, due to surface tension effects and increased temperatures, the thin catalyst layer breaks down into discrete nanoparticles that serve as the catalysts for the reaction [20]. Preferentially, at these

catalyst sites, the silane vapor decomposes into silicon and hydrogen gas at approximately 350ºC, and subsequently a liquid AuPd-silicon alloy at the eutectic temperature, or approximately 542ºC, is formed (where this value was calculated based on Au-Si (T_e=363ºC) and Pd-Si (T_e=810ºC) phase diagrams (Appendix 9.2) and the $Au_{0.6}Pd_{0.4}$ composition as no tertiary phase diagram exists) [7, 31]. During the synthesis process, the catalyst-silicon alloy continues to absorb silicon until supersaturation is reached. The actual silicon nanowire synthesis occurs as silicon precipitates from the silicon-supersaturated alloy to form a one-dimensional single crystal nanostructure at the liquid-solid interface [7, 31]. Based on the simulation models, this precipitation reaction appears to take place between the eutectic temperature and approximately 700ºC. The thermal bounds of this reaction are discussed in the results section, but it is important to remember that in this work the surface temperature of the MEMS structure was never determined experimentally due to the lack of appropriate tools. The limitation of currently available tools is the dimension of the spot size. In all cases the spot size is larger than the width of the MEMS structure causing the tool to average the temperature reading over a temperature range extending from room temperature to synthesis temperature or hotter. Therefore, all temperature values cited in this work are generated based on simulations, known properties of the materials involved in the reaction and visual observations of the post VLS synthesis results.

3.3 Results & Discussion

The series of images in Figure 3.7 illustrate the viability of the process. A

number of key observations demonstrate the success of the process: (1) it appears that the VLS process does successfully take place within a localized heating environment proving that a confined synthesis region without catalyst patterning is possible, (2) direct micro-to-nano integration is clearly a feasible method, and (3) localized heating is an acceptable post-CMOS process as cold chip regions remain unaltered by the reaction.

Silicon nanowires produced in this process range from 20-100nm in diameter and depending on the growth time, surface temperature and chamber pressure are measured at up to 29μm long. Nanowire aspect ratios achieved in this process can easily reach 100 but may reach 500 for the longest nanowires. Noticeably, within any synthesis region, nanowires of varying diameter and length exist. Both nanowire density and nanowire diameter is governed by the breakdown of the catalytic thin film. Within the localized growth region nanowire densities can reach 45 nanowires per square micron as the nanowires overlap each other and take up space out of plane. Peak growth rates of up to 1.5μm/min have been demonstrated. A TEM based analysis of the attributes of the silicon nanowires within the growth region is presented in Chapter 5.

The yield of the localized synthesis process, defined solely based on successful silicon nanowire synthesis is over 90%, pointing to the robustness of the VLS process even in a localized heating environment. The main contribution to the non-success of the synthesis process is debris on or around the MEMS structure's surface, introduced either during the fabrication or packaging process, which alters the I-V characteristic

of the structure.

3.3.1 Visualization of Process Results

The attributes and features of the process, based on SEM analysis of post VLS samples are now discussed in detail. Figure 3.7 presents a number of key process results and attributes. The localization of the nanowire synthesis region is clearly demonstrated while the localization of the heating is evident as well. In Figure 3.7(a) a top view of a fixed-fixed 100μm long and 5μm wide polysilicon MEMS structure with silicon nanowire synthesis localized to the central 35μm is seen. The oblique view in Figure 3.7(b) illustrates that the center of the growth region exhibits shorter nanowires than do neighboring regions to the left and the right. It is believed that this structure has self-buckled downward to the substrate during the synthesis process due to compressive stresses generated by the thermal expansion during the heating process [59]. As a result, the temperature at the center of the bridge decreased as the heat dissipation rate to the substrate, locally, increased and the nanowires in this area grew at a slower rate [21]. In Figure 3.7(c), the localized synthesis process took place on a <111> oriented MEMS structure yielding what appears to be straighter nanowires, probably with fewer defects due to the lattice match between the synthesis surface and preferred nanowire growth direction, possibly suggesting an epitaxial contact [22, 31]. This image also clearly illustrates the temperature dependence of the VLS reaction as nanowire length changes with location. Figure 3.7(d) illustrates that variations of the U-shaped design, such as V-shaped structures in this case, also meet the requisite conditions for thermal stress relief and are therefore suitable for the

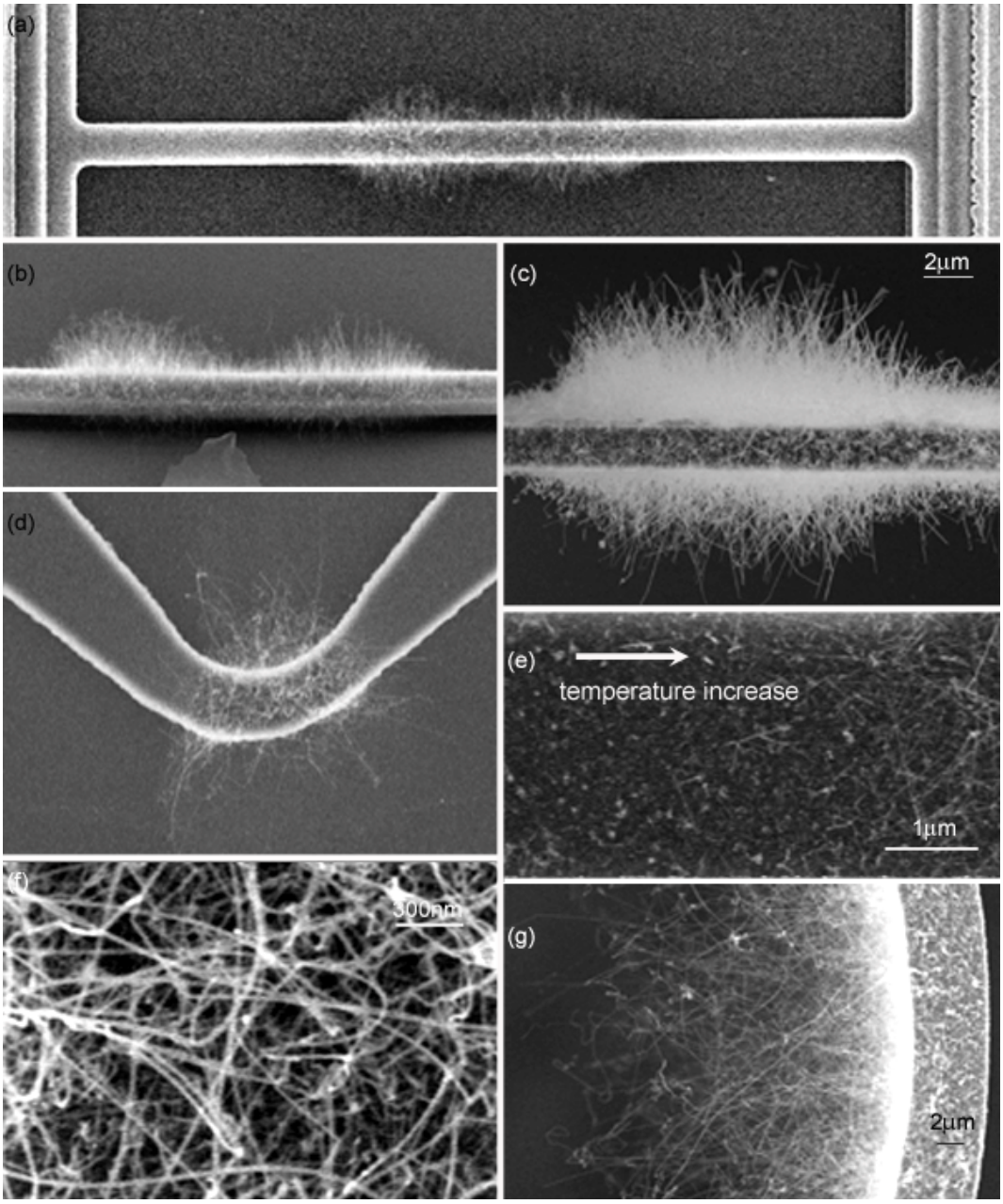

Figure 3.7. Silicon nanowire (SiNW) growth following localized VLS process. (a) A 100μm-long polysilicon MEMS structure with silicon nanowire growth centrally localized to 35μm of the structure. (b) An oblique view of the localized growth in (a) illustrating shorter nanowire growth at the center of the MEMS structure as a result of the buckling of the structure towards the substrate and the ensuing locally increased heat dissipation rate. (c) Localized SiNW growth on a <111> oriented MEMS structure. (d) Localized SiNW growth on a V-shaped structure of decreasing cross-section at the apex. (e) A view of the growth-no-growth interface along a MEMS structure due to thermal boundaries of the VLS process. A gradual onset of SiNW growth is seen with a change in temperature. (f) SiNW growth on the surface of the MEMS structure, illustrating the high nanowire density within the growth region. (g) SiNW growth from a semicircular SCS MEMS structure. The free ends of the nanowires are seen to kink and bend greatly.

localized synthesis process. In fact, the changing width of the structure (the narrowest portion is at the apex (2μm wide)) assists in further localizing the heating to this region of the structure. Figure 3.7(e) provides a top view of the growth-no-growth interface with the temperature value increasing from left to right, providing a clear boundary of the location along the MEMS structure's surface where the temperature was sufficient to support the VLS mechanism. While it is clear that the heating is responsible for some changes on the surface, the sensitivity of the VLS process to temperature is clearly illustrated. A high-density growth region is illustrated in Figure 3.7(f), exemplifying the consequences of the randomness associated with the breakdown of the thin film layer, thus dictating nanowire diameter and growth region density. Nanowire synthesis along a semicircular MEMS structure is seen in Figure 3.7(g). The longest nanowires are approximately 23μm long achieved as a result of 40 minute long synthesis process at a chamber pressure of 239mTorr to demonstrate a peak synthesis rate of 0.57μm/min. Within this or any growth region, however, a wide range of growth rates exists as governed by the local surface temperature. The relationship between the synthesis chamber pressure and growth rate is also examined in this context. Figure 3.8 illustrates a growth rate versus pressure relationship based on experimental results, where the growth rate calculated for each sample represents the peak growth rate which is determined by fitting the growth region to a parabola with a vertex at the sub-region of maximum nanowire length and then measuring the distance from the MEMS structure to this location. The growth rate was determined by dividing the nanowire length by the

growth time. The nanowire length measurement is subject to a ±2μm error as the origin of the nanowire is at times difficult to accurately locate. Length measurements were conducted to unconstrained nanowire growth regions only. There appears to be a fairly strong correlation between pressure and growth rate and a substantial decrease in growth rate at low pressures. The data further suggests that the growth rate is maximized at total chamber pressure of 270-330mTorr, or SiH_4 partial pressure of 27-30mTorr but does show a reduction with an additional increase in pressure. Figure 3.8, however, does not consider the effect of temperature on the growth rate and omitting this effect may distort the trend. It is difficult to tie this data with pressure

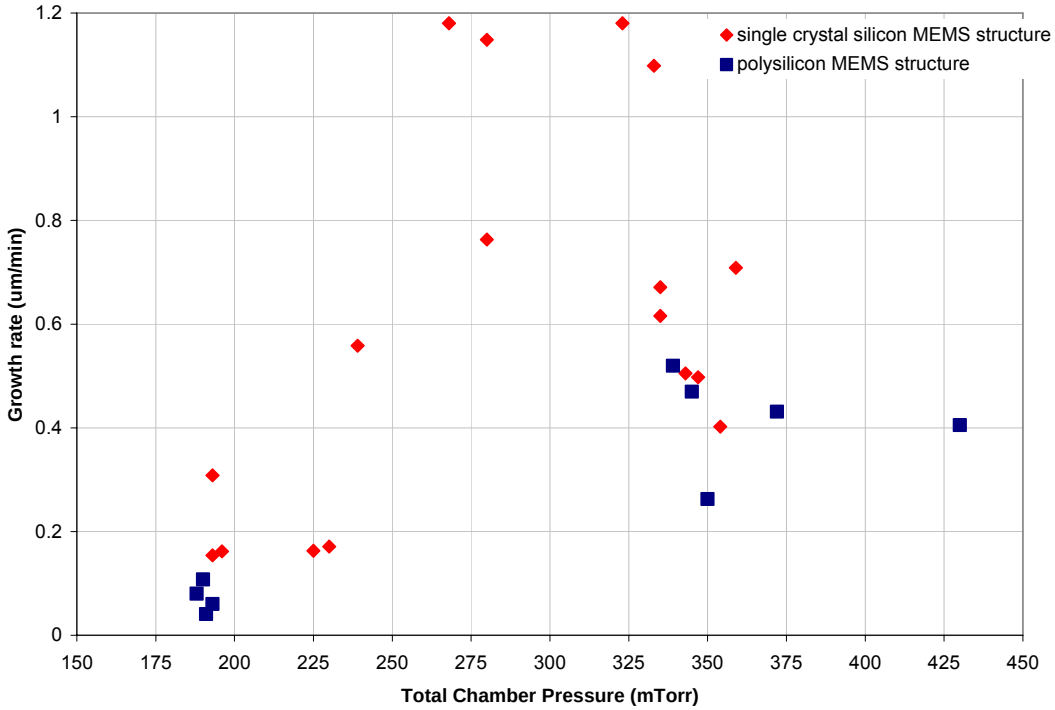

Figure 3.8. Experimental correlation between nanowire growth rate and chamber pressure. The data suggests an increase in growth rate in between 270mTorr and 330mTorr and a significant reduction in growth rate with chamber pressures below 200mTorr. This plot does not consider the effect of temperature.

requirements from the literature since in very few instances is the VLS reaction conducted at such low pressures while in addition, growth rate is seldom addressed. Reference [23], however, does suggest an increase in growth rate with increased pressure and reference [12] documents a 900 time increase in growth rate over a 130ºC temperature change. It may be therefore suggested that the relation in Figure 3.8 would become further linearized if all growth rate measurements were conducted at the same growth temperature. Synthesis in a very low pressure environment (<200mTorr), while possible, eliminates the very rapid turnaround time that the localized VLS process is capable of. While the peak growth rates per growth regions are 1-1.2μm/min, the absolute peak rate realized by this process, determined based on the longest nanowire in a specific growth region is 1.4-1.6μm/min. Finally, the synthesis surface appears to be independent of pressure, as both single crystal silicon and polysilicon MEMS structures show similar growth rates as a function of pressure.

3.3.2 Thermal Attributes of Process

As previously discussed, the localized silicon nanowire synthesis process is a strong function of local temperature, and there appears to be an ideal temperature window at which the reaction takes place. In other words, if the temperature is too low or too high the VLS reaction will not take place. The minimum threshold temperature required for this VLS reaction to take place is established by the eutectic temperature of the catalyst-silicon alloy (AuPd-Si). At the same time, it is also observed that there is a maximum temperature beyond which the reaction will not take place. Although it is not possible to directly measure temperature at specific

regions of the MEMS structure, the predicted parabolic temperature distribution through the MEMS structure along with the resulting synthesis distribution also provides a clue to the upper thermal bound. For example, Figure 3.9 illustrates silicon nanowire growth at two off-center locations while no growth is evident at the center of the MEMS structure. It is surmised that the temperature in the region between the growth regions was too high for the VLS reaction to take place while the

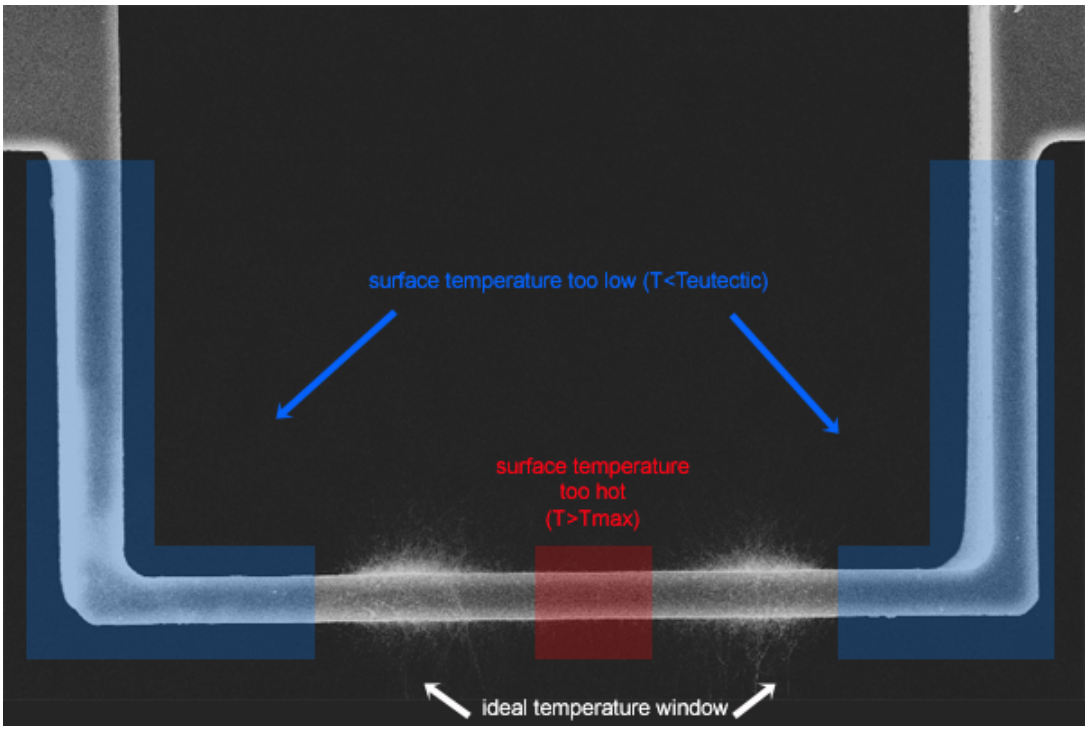

Figure 3.9. Temperature dependent growth locations. Two independent silicon nanowire growth regions occurring within the ideal temperature window required for the VLS reaction. The center temperature (red region) is too high while the blue regions mark regions too cold for the reaction to take place.

temperature in the regions beyond the growth regions was too low. As predicted by the parabolic temperature distribution, the two off-center locations are at the same temperature and represent the ideal synthesis temperature. The extent of each growth region in this case is shorter in length than the centered growth of an identical MEMS

structure due to the more significant temperature gradients expected from a parabolic distribution when moving away from the geometric center of the structure. In fact, the extent of a centered growth region covers 20-40% of the MEMS structure's surface length while off-centered growth regions cover only 8-15% of the total length [68]. Figure 3.10 compares the experimental I-V relationships and resulting growth region for two identical polysilicon MEMS structures (identical geometry and resistance) subject to identical synthesis conditions except that the applied voltage to the structure in Figure 3.10(c) is 0.11V greater than the voltage applied to the structure in Figure 3.10(b). As suggested by the simulation, even a small difference in the applied power changes the maximum surface temperature of the MEMS structure and causes a shift from a single centered growth region to two distinct off-centered growth regions. A centrally localized growth region is therefore only an indication that for a specific sample, the hottest temperature region of the MEMS structure matches the thermal requirements of VLS process. This result does provide an additional control parameter to the process. That is, by carefully controlling the level of heating, the location of the growth region along the MEMS structure can be accurately determined. This may have an implication or application when designing more complex micro-to-nano systems.

The upper thermal bound of the VLS reaction under the unique conditions explored in this work may be due to the evaporation of the catalyst or diffusion of the catalyst into the bulk once a certain critical temperature is reached. The diffusion hypothesis may be dismissed as studies of thin AuPd films on silicon

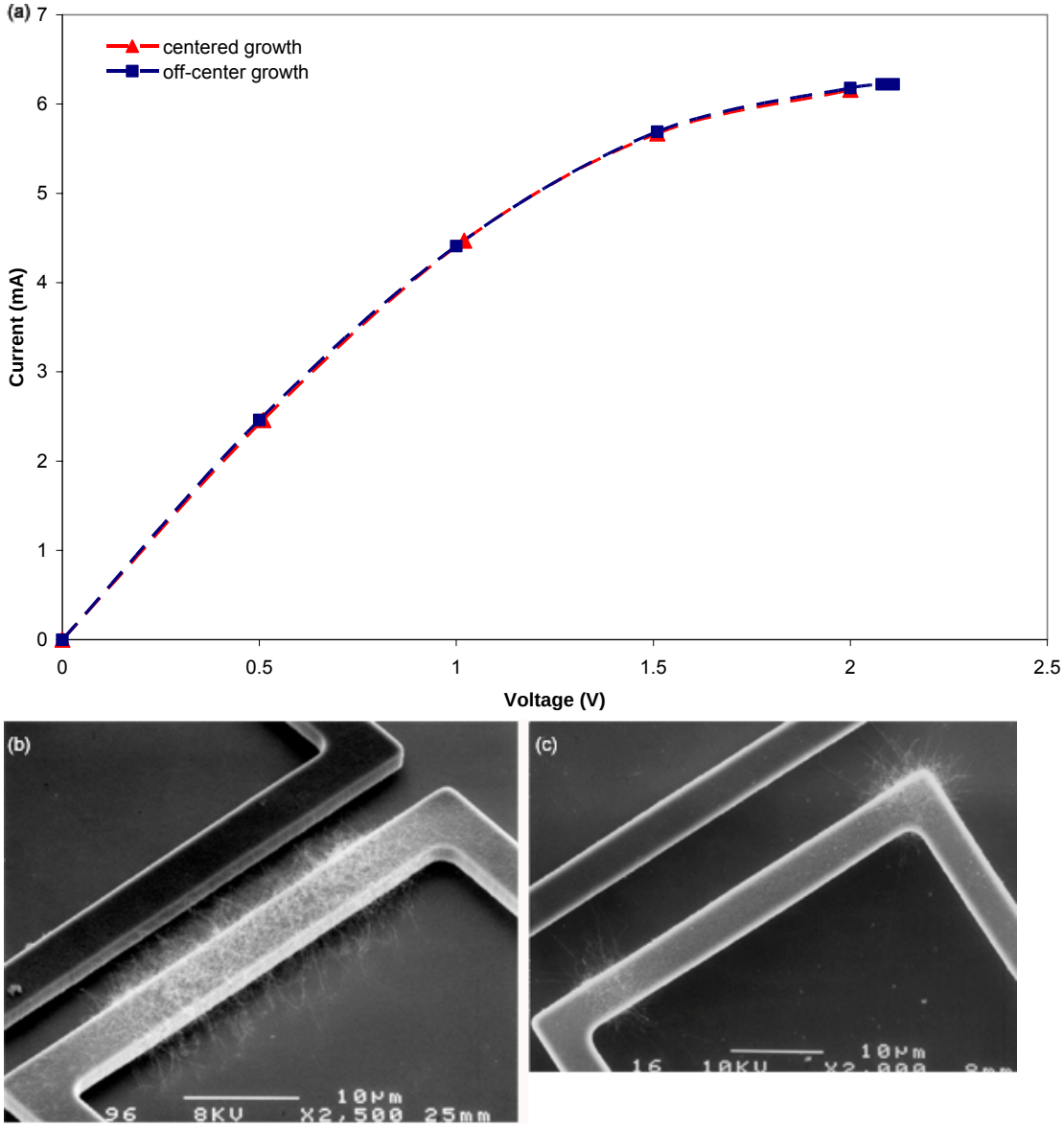

Figure 3.10. Tying experimental MEMS structures' I-V data with silicon nanowire growth. (a) Experimental I-V curves of two identical, neighboring MEMS structures (R=190Ω). During the VLS process the applied power to the structure in (b) was 2V and 6.16mA while 2.11V and 6.22mA was applied to the structure in (c). The structure in (b) exhibits centered growth while the structure in (c) exhibits two comparably short off-centered growth regions.

substrates with a native oxide present at up to 620ºC suggest that palladium readily diffuses through the oxide while gold aggregates to form 3D particles and tends to remain on the surface [69, 70]. Another plausible explanation could be that the

experimental conditions favor another reaction, such as the localized deposition of polysilicon, rather than single-crystal silicon nanowire growth, as seen in Figure 3.11 and demonstrated in [71]. The upper thermal bounds of the reaction could also be based on the eutectic diagram. With the assumption of locally constant temperature throughout the synthesis period, the amount of silicon in the alloy required to reach supersaturation, or the liquidus line composition in the phase diagram, increases with increasing temperature. It could be that the experimental silane flow parameters coupled with the increased silicon composition requirements cannot meet the supersaturation requirements and hence no synthesis takes place.

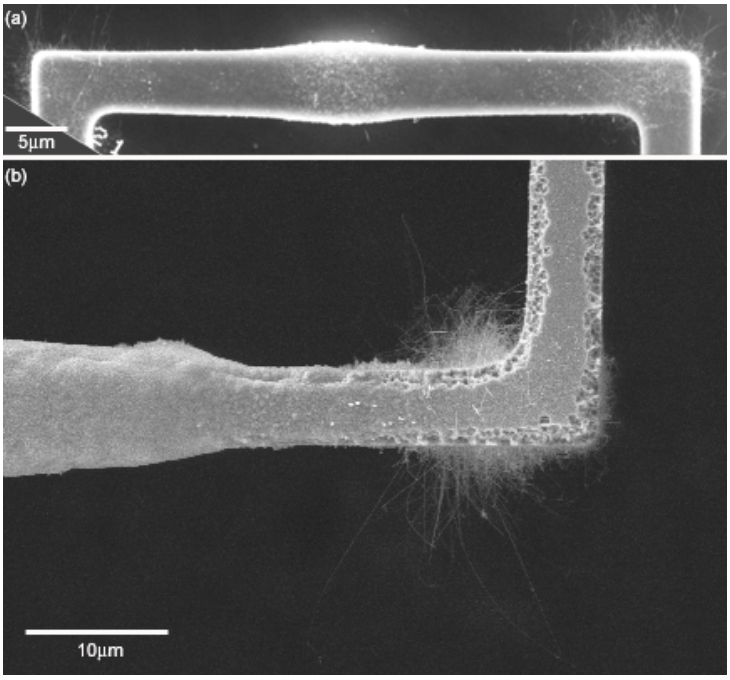

Figure 3.11. Polysilicon deposition along high temperature regions of the MEMS structure. (a) Polysilicon deposition at the center of a polysilicon and (b) SCS MEMS structure respectively. Off-centered silicon nanowire growth regions are visible as well.

It is often observed that the growth regions are not aligned with the geometric center of the MEMS structure as would be suggested by the simulated parabolic

temperature distribution. This misalignment is clearly visible when off-centered growth takes place. These observations suggest that the hot spot is slightly skewed away from the geometric center of the structure. The shifting of the hot spot results from a second-order thermoelectric effect known as the Thomson effect which appears when a temperature gradient exists along a current path. The Thomson effect contributes a linear heat generation term to the quadratic volumetric heat generation term (Equation 3-2). This additional term develops as a result of carriers moving from warmer to cooler regions [62, 72-74]. The shift of the central hot spot was measured to be between 3-15% as determined by comparing the center of the MEMS structures, as defined by the growth region to the geometric center. This effect is clearly seen in the U-shaped structures and specifically in off-centered growth samples. The hot spot of the MEMS structure is always shifted towards the high voltage end of the MEMS structure. An example of the Thomson effect is illustrated in Figure 3.12 and 3.7μm shift of the hot spot (red line) away from the

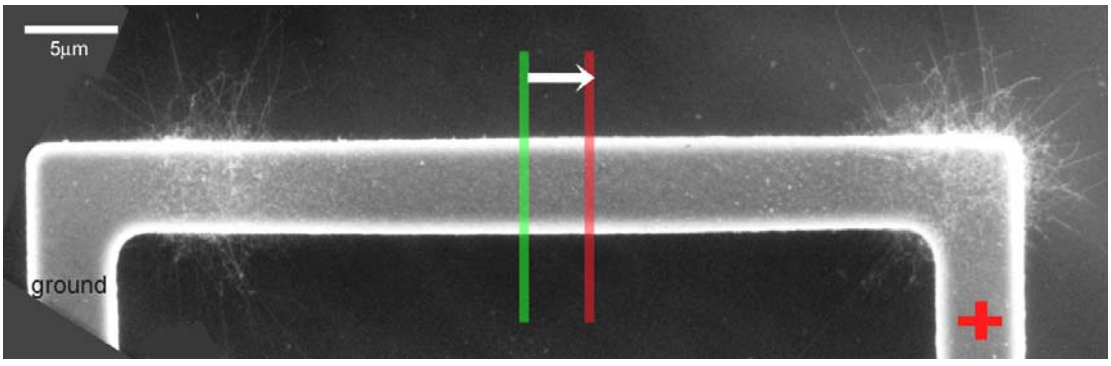

Figure 3.12. Illustration of the Thomson effect. A polysilicon MEMS structure with two off-centered growth regions misaligned with respect to the geometric center of the MEMS structure (green line). The heated center of the beam (red line) is shifted 3.7μm towards the high voltage end due to the Thomson effect and the resulting growth regions are symmetric with respect to the red line.

geometric center of the MEMS structure (green line) is noted. Although slight, the hot spot shift is directly related to a shift in the growth region's location, and must be accounted for when designing more complex micro-to-nano systems.

3.3.3 Other Considerations & Observations

The extent of the nanowire growth through the length of the MEMS structure was previously discussed. The extent of the nanowire growth through the width of the MEMS structure is governed only by the presence of the catalyst since the temperature does not vary through the cross-section of the structure. Since the catalyst deposition step is not lithography bound, the catalyst is present chip-wide yielding a constant nanowire density through the width of the MEMS structure. The thin catalyst deposition generally covers only the top surface of the MEMS structures; however, even a slight tilt of the chip results in some sidewall deposition, which leads to nanowire growth originating from the upper most sidewall areas of the MEMS structure. The role of the synthesis surface in this process was speculated to be minimal and in fact the results illustrate no dependence on the synthesis surface. Visually, images throughout this work depict localized silicon nanowire synthesis on both single-crystal silicon and polysilicon MEMS structures with no glaring difference. In addition, Figure 3.8 shows consistent behavior as a function of pressure.

Observation of the free tips of the silicon nanowires often illustrate extreme kinking and bending (Figure 3.7(g)). Since the VLS process dictates that the newest portion of the nanowire is always located just below the liquid alloy, this behavior

appears to be linked to conditions during the termination of the VLS process and possibly the temperature change and the halting of the vapor phase supply. The literature suggests that changes in the VLS synthesis conditions during the process that lead to instabilities at the liquid-solid interface may introduce irregularities during nanowires growth [6]. Two cases were examined in this context: the termination of the SiH_4 supply prior to cutting off the power supply (at high local temperature) and the termination of SiH_4 flow after cutting off the power supply (at room temperature). It was found, however, that the different VLS process termination conditions do not appear to significantly alter the growth phenomena at the free end of the nanowire.

Controlling the nanowires' diameter is important towards achieving uniform properties across the growth region and is essential for certain devices and sensing applications. The mask-less thin film deposition process and the aggregation of the thin film into nanoparticles yields a non-uniform distribution of nanoparticles and hence nanowire diameter. Patterning nanoparticles is not a practical approach; however, dispensing prefabricated nanoparticles does provide the means for easily placing uniform catalyst particles onto the growth surface. Gold nanoparticles (Ted Pella), 20nm in diameter and a concentration of $7x10^{11}$ particles/ml were dispensed from solution onto the chip and heated slightly to evaporate the liquid. While the thin film deposition process places the catalyst primarily on the top surface of the MEMS structures, deposition from solution places the catalyst on the top surface as well as the sidewalls. The results are seen in Figure 3.13 and illustrate significant growth

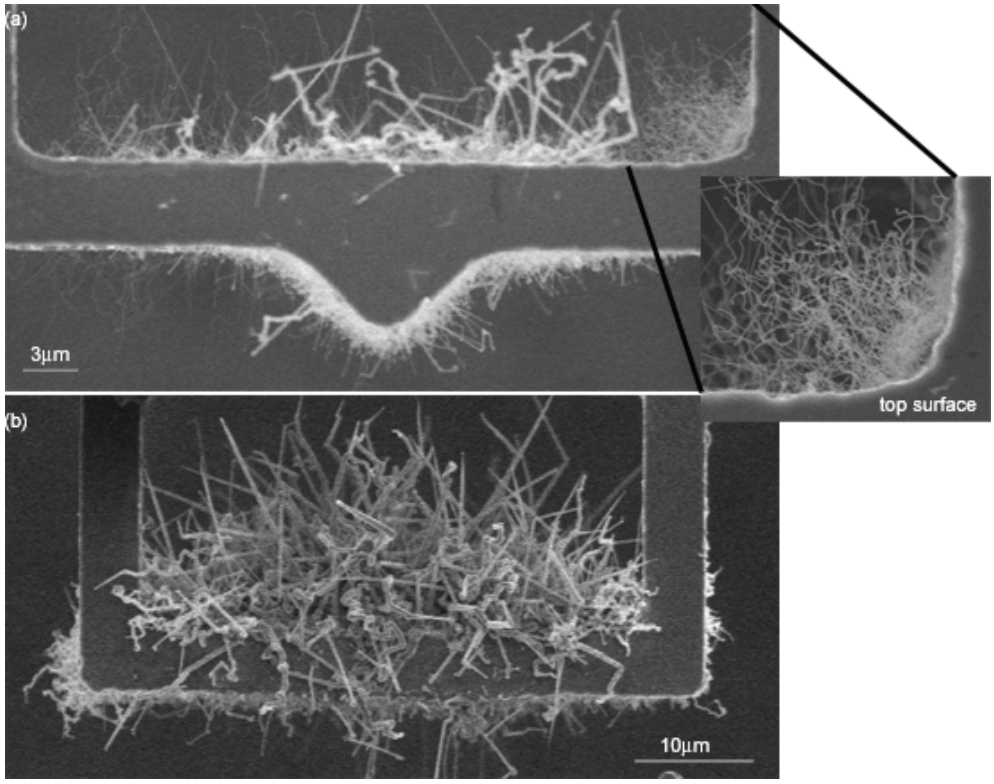

Figure 3.13. Prepared-gold-nanoparticle mediated localized silicon nanowire growth. (a) A significant portion of the growth region appears on the sidewall rather than the top surface of the MEMS structure as the position of solution dispensed catalyst is no longer constrained to the top surface of the MEMS structure. The inset illustrates very uniform diameter nanowires along the sidewalls. (b) Another example of significant sidewall growth and minimal top surface growth. The diameter of the nanowires, compared to the inset, for example, suggests that many of nanoparticles have clustered together.

along the sidewalls rather than the 'typical' top surface growth and at times (inset) better uniformity of nanowire dimension. Since the nanoparticle distribution is random, the extent of the growth region, although localized, is wider. Often, clustering events of the nanoparticles result in larger than expected nanowire diameter. Surface treatment processes have been shown to enable the further localization and separation of the nanoparticles [22]. Although such processes are very effective, they were not attempted in conjunction with this process in order to maintain the simplicity of the process.

3.4 Summary

A method for the localized synthesis of silicon nanowires enabling the direct and site-specific micro-to-nano contact during the nanostructure synthesis process is developed in this chapter. This technique utilizes of a top-down process (MEMS structures) followed by a bottom-up process (VLS synthesis), a twist on the traditional practices. This process allows for a simple, quick and high yield technique.

The design of the MEMS structures is critical for realizing controlled localized heating and is further a consideration for taking full advantage of this direct integration process as the contacts to the MEMS structures also provide direct access for electrical characterization and device testing purposes for any system assembled in this manner. The localization of the required heating to portions of growth structure provides an additional and unique level of control over alternative nano-to-micro integration processes. In addition to its practicality, this process also offers a unique view of the VLS process as a complete temperature range is explored in a single experiment. While AuPd is not the traditional VLS catalyst, it nonetheless functions very reliably to yield consistent results. Finally, the localized heating process could be easily automated to further streamline the process. In fact, all that is necessary is control software which increments the voltage while measuring the current and evaluating the slope of the I-V curve. Once the slope is equivalent to zero, the controller maintains the applied voltage for a predetermined time period depending on the process requirements.

4 Self-Assembly of a Micro-to-Nano System

4.1 Introduction

While conventional nanowire assembly techniques require post-synthesis manipulation and contact formation, the process described here enables a simpler, in-situ assembly method. The localized synthesis process can be easily utilized to link together multiple MEMS structures with silicon nanowires [75]. Experimentally, two MEMS structures are positioned in close proximity to each other and the synthesis process is initiated on one of the structures as previously described. Due to their unique functionality, the MEMS structures will be referred to, from here on, as the 'growth' structure and the 'secondary' structure as shown in Figure 4.1. The application of a localized electric-field during the synthesis process produces noticeably improved nanowire order, alignment and organization while transcending the gap between two MEMS structures [76]. While others [53] have commented about the tediousness the electric-field assisted growth method due to the required electrode patterning, this method perfectly complements the process presented in this work as the MEMS structures serve as both the growth/secondary structures and electrodes.

4.2 A Two-Terminal, Self-Assembled Micro-to-Nano System

The two-terminal, self-assembled system consists of two closely spaced MEMS structures linked together with silicon nanowires. More specifically, two identical MEMS structures spaced 4 to 10μm apart were lithographically defined, such that either structure could serve as the 'growth' structure, while the second structure serves as a location for the secondary contact and hence the 'secondary' structure designation. In other words, the result sought in this experiment is localized nanowire synthesis to bridge a gap between microscale structures. Once the synthesis process is complete, each end of a nanowire may be attached to a different MEMS structure as a result of a self-assembly process such that no additional manipulation of the nanowire into place is required. A schematic of the experimental setup is illustrated in Figure 4.1. The nanowire synthesis process takes place on the hot,

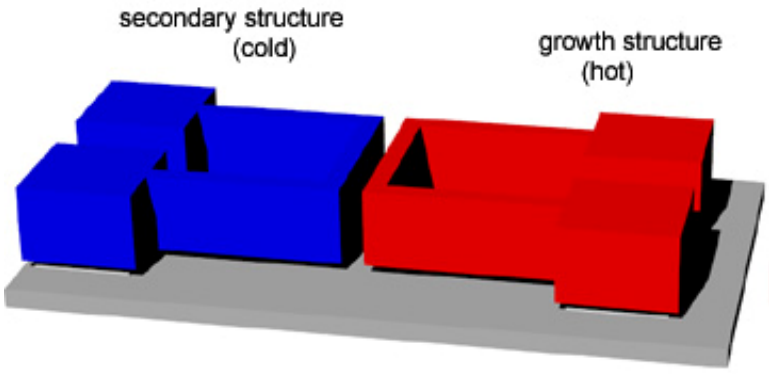

Figure 4.1. Experimental setup for self-assembly of silicon nanowires among multiple MEMS structures. Two opposing MEMS structures; one (red) serving the growth structure as it is locally heated, while the other (blue) remains at room temperature and serves as a natural termination point for the VLS process.

'growth structure' while the opposing cold, 'secondary structure', remains at room temperature, and serves as the end point for the growth process since the temperature

requirements necessary to sustain the VLS reaction no longer exist at the secondary structure location.

4.3 Electric-Field Assisted Growth

While the experimental setup detailed above permits the successful localized synthesis of silicon nanowires to yield a two-terminal, self-assembled system, the application of the local electric-field provides the means to improve nanowire organization and alignment across the gap as the nanowires appear to be guided by electric-field lines.

4.3.1 Microscale Design Considerations

In order to study the response of silicon nanowires to the presence of a localized electric-field, the two MEMS structures setup is again utilized. As the secondary structure is positioned in close proximity to the growth structure's location, a local electric-field may be exclusively set up between the two structures. The design of the secondary MEMS structure may be identical to the growth structure or may alternatively take another configuration as the design constraints which are placed on the growth structure do not apply to the secondary structure. For this specific set of experiments, the MEMS structures' design particularly benefits from the use of SOI wafers with a device layer thickness greater than the width of the gap defined between the MEMS structures as inhibiting effects resulting from nanowire interaction with the substrate during the synthesis process are eliminated [44]. In other words, this setup permits the nanowires to contact the secondary structure prior

to becoming sufficiently long to reach and interact with the substrate.

4.3.2 Experimental Setup

The local electric-field is created by placing the secondary structure at a constant negative potential with respect to the growth structure, thereby creating a voltage drop from the growth structure directed towards the secondary structure. The secondary structure, therefore, does not experience resistive heating effects. The secondary structure is connected to a power supply through a large resistance resistor (typically10MΩ) to prevent a significant voltage drop across the nanowires once a contact to the secondary structure is made. The experimental setup is schematically depicted in Figure 4.2. Additionally, for the purpose of this experiment, the

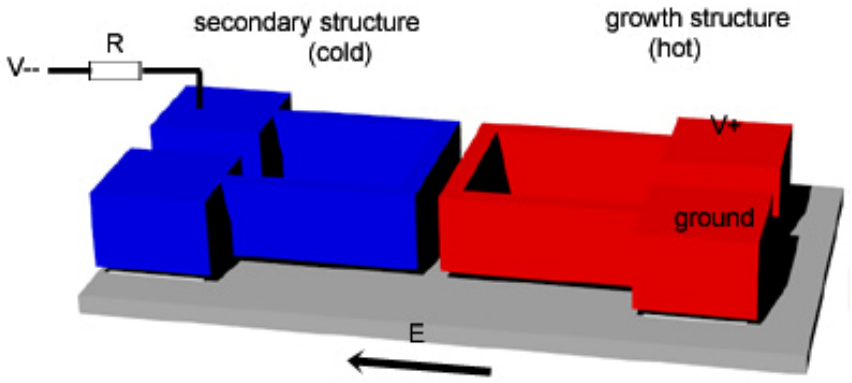

Figure 4.2. Experimental setup for electric-field assisted growth and self-assembly of silicon nanowires. The growth and secondary structures serve as both, hot and cold structures respectively as well as functional electrodes for the application of a localized electric-field.

nanowires are strategically synthesized using only silane as the vapor source without the introduction of a dopant gas into the flow stream. As such, it is ensured that synthesized nanowires are essentially electrically intrinsic and the observed response

may be considered a baseline response.

4.3.3 Attributes of a Localized Electric-Field

The magnitude of the voltage drop and the distance between the two MEMS structures can be used to approximate the strength of the electric-field. In all the experimental cases, the local horizontal electric-field is slightly non-uniform due to the applied voltage drop across the growth structure. More specifically, the non-uniformity occurs due to a linear voltage drop which takes place along the growth structure leading to a correspondingly linear decrease in the electric-field strength. Therefore, the corner closest to the high-voltage end is subject to a slightly stronger electric field than does the corner near the grounded end. For example, if 10V are required to sufficiently heat the growth structure and the structure is U-shaped with three 50μm-long segments, than the voltage drop along the growth structure is 0.067V/μm, and the growth structure's contribution to the electric-field at the corner closest to the high voltage supply will be twice as large as that of the other corner. Vertically, the electric field is uniform and perpendicular to the MEMS structures while fringe field effects are expected along the top, bottom, left and right edges. Electrophoresis, however, has been shown to take place regardless of the homogeneity of the field [77].

Without consideration of local field enhancement effects, the experimental setup bounds the electric-field strength from above and below. The maximum field strength is governed by the maximum voltage drop at the location of minimum separation between the structures. More specifically, the maximum voltage input

comprises of the maximum voltage which may be applied to the growth structure while meeting the thermal requirements of the VLS process and maintaining the structural integrity of the growth structure and the maximum voltage which may be applied to the secondary structure as governed by the dielectric breakdown value of the insulating oxide layer which separates the anchors of the MEMS structures from the substrate. The latter is always greater than the former under typical experimental conditions. The significant potential difference between the structures renders the voltage drop through the growth structure inconsequential for electric-field strength calculations. The minimum electric-field strength is approximately zero, determined by setting the applied voltage to the secondary structure to half the voltage applied to the growth structure.

Although the electric-field strength is inversely proportional to the width of the gap between the MEMS structures, minimizing the width of the gap was not an effective method of increasing the strength of the field due to constraints placed by lithography as well as the resulting minimization in the length of the nanowires which is less desirable for many applications. Instead, electric-field enhancements were realized by manipulating the shape and configuration of the secondary structure. The concept utilized here is based on antenna or tip effect where charge accumulation at isolated locations contributes to enhanced electric-fields [78].

4.3.4 Theory & Simulation

FEMLAB® finite element modeling software was used to quantify electric-field enhancement near sharp tips and corners that occurs due to charge accumulation.

Since the intensification is shape dependent, a localized effect is expected. The analytical solution to this problem suggests that at the limit of an infinitely sharp tip, the electric-field strength is infinite [79]. More specifically, considering a wedge representation for the 2-dimensional case, where the sharpness of the wedge is a function of the wedge angle, θ_0, and a very sharp wedge is defined as $\theta_0 << 1$, the relationship between the electric-field and *r* is expressed in Equation 4-1, where *r* is the distance from the vertex of the wedge, and *r* approaching zero is the limit of interest. A relation between the electric-field and *r* for the 3-dimensional case, where now, a very sharp cone is considered, has been formulated as well (Equation 4-2) [79]. These expressions clearly suggest that electric-field strength increases significantly in the vicinity of a sharp tip.

$$E \propto \frac{1}{r^{1/2}} \qquad \text{Equation 4-1}$$

$$E \propto \frac{1}{r} \qquad \text{Equation 4-2}$$

$$(r \rightarrow 0,\ E \rightarrow \infty)$$

Considering the case of two identical opposing MEMS structures, uniform and constant electric-field strength is expected in the gap while simulation is utilized to determine the electric field enhancement at and around corner locations. Working with experimental values where, for example, the corner of the growth structure is placed at a 6V potential and the secondary structure is placed at -20V potential, uniform electric-field strength of 5.2V/μm is expected, and confirmed by simulation, across a 5μm gap. The 3D finite element model further predicts a peak electric-field

strength value of approximately 7.5V/μm, a 1.4 time increase in field strength, at the

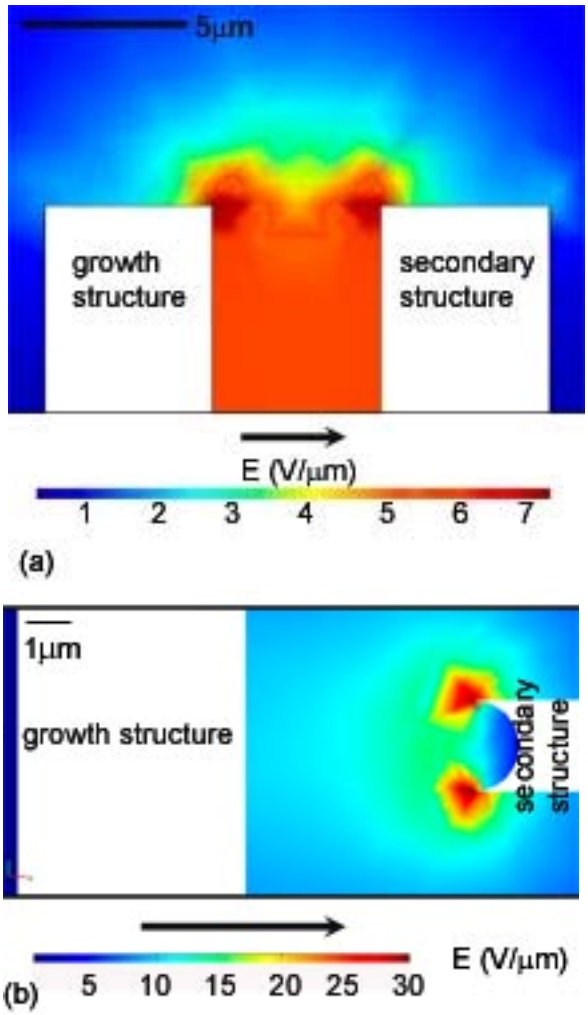

Figure 4.3. Finite element modeling of electric-field enhancement. (a) Investigation of electric field enhancement at corner locations between two MEMS structures 5μm apart. The calculated electric field in the gap is estimated to be 5.2V/μm, while simulation suggests a peak electric field value at each corner of 7.5V/μm. (b) Electric field enhancement between the growth structure and a sharp-tip crescent shape secondary structure. Significant field enhancement in the vicinity of the tip is seen as the peak simulated value is 30V/μm while the experimental value is 13V/μm.

corner and further illustrates the degradation in electric-field strength with increasing distance from the MEMS structures thus finely defining the fringe-field effect in this region (Figure 4.3(a)). Within 1μm away from the corner, the electric-field intensity drops to approximately 4V/μm and at a distance of 2μm the electric field strength

drops to approximately 2V/μm.

As expected, a more pronounced enhancement results with the use of sharper edge MEMS structures. The finest tip structure microfabricated in this process is a crescent shaped structure forming a tip with a 30-60º wedge angle. Experimentally, for a sharp secondary structure, placed at -60V, located 5μm away from the center of a growth structure placed at 5V, the model predicts a local electric-field, approximately 30V/μm at its strongest point, or about twice as large as the directly calculated value of 13V/μm without consideration of field enhancement effects (Figure 4.3(b)).

4.4 Results & Discussion

4.4.1 A Basic Two-Terminal Micro-to-Nano System

Figure 4.4 illustrates examples of localized silicon nanowire growth linking together multiple MEMS structures to yield a two-terminal-self-assembled system. The confinement of the nanowire growth to the growth structure is evident as the surface of the secondary structure is clean. The termination of the synthesis process upon contact with the secondary structure is evident as well. This phenomenon is established by comparing the lengths of nanowires growing towards the secondary structure with the length of nanowires growing away from the secondary structures; the length of the latter is determined by the length of the gap while the length of the former is a function of the synthesis time. The opposing semicircular MEMS structures in Figure 4.4(a) and the zoomed-in view in Figure 4.4(b) further validate this observation as the nanowire length changes with the width of the gap. In Figure

4.4(c-d), additional examples of the two-terminal micro-to-nano self-assembled system clearly illustrate the termination point of the growth process at the secondary

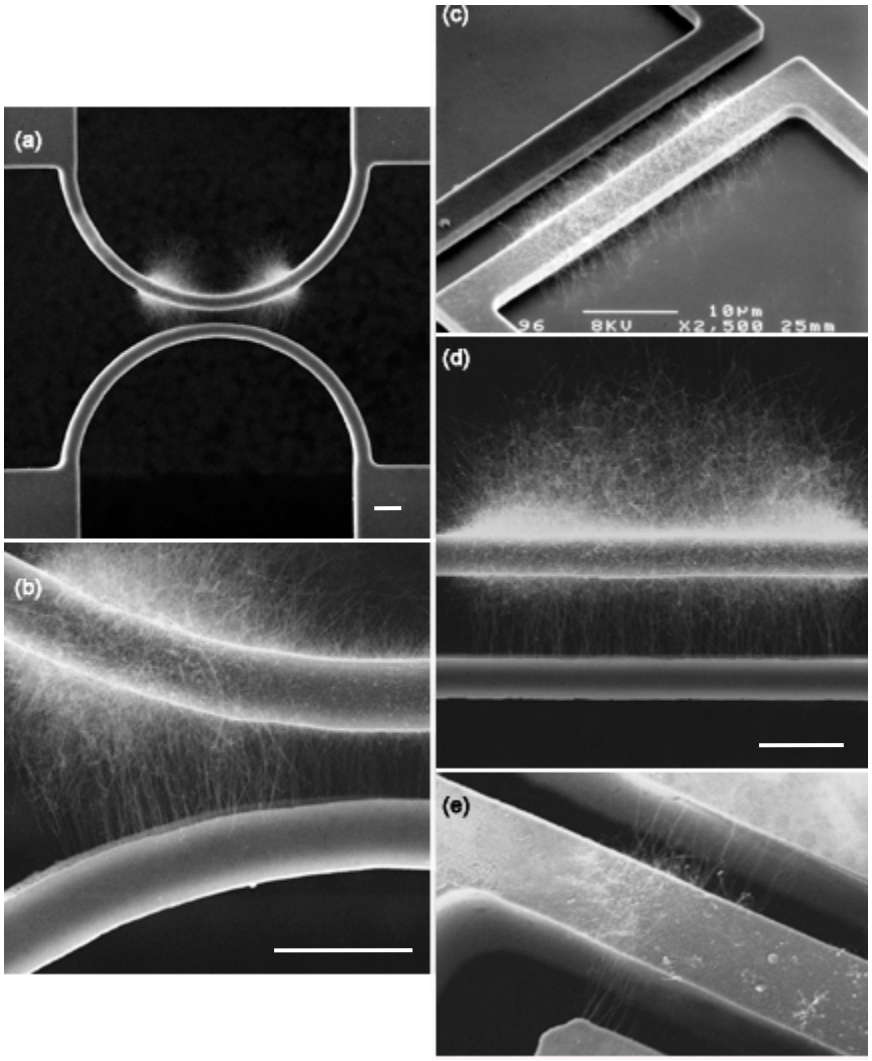

Figure 4.4. The self-assembly of silicon nanowires to link together multiple MEMS structures. (a) SiNW growth between two semicircular SCS MEMS structures. The growth structure is the top structure. The length of the nanowires changes with the length of the gap thus confirming that the VLS process terminates at the cold, secondary structure. Nanowires growing away from the secondary structure (top of image) are significantly longer than nanowires in the gap. (b) Close in view of nanowires in the gap (the growth structure is the top structure). (c) Silicon nanowire growth between two U-shaped polysilicon MEMS structures (the bottom structure is the growth structure). (d) Silicon nanowire growth is significantly longer away from the gap than within the gap (growth structure is the top structure). (e) The growth structure is the center structure and nanowire growth to two independent secondary structures is observed. (All scale bars are 10μm.)

structure for nanowires bridging the gap. Figure 4.4(e), on the other hand, shows the flexibility of the process with a central growth structure and two secondary structures thus doubling the output of the localized synthesis process.

While this work is primarily focused on horizontal nanowire synthesis, vertical nanowire growth to link together vertically offset MEMS structures has also been demonstrated. The MUMPs™ process is particularly suitable for this process and nanowire growth contacting the structural layer above it as well as the ground layer below have been demonstrated (Figure 4.5). However, specifically in the case of vertically overlapping structures, a limitation of this process is the modified and as such enhanced heat dissipation regime of the growth structure. Nonetheless, nanowires that would under standard synthesis conditions tend to remain in-plane are seen to grow vertically in the vicinity of the vertically offset secondary structure. This approach may be advantageous, however, as it minimizes the lateral die space requirements.

The yield of the localized synthesis and self-assembly process was calculated to be over 60%, where yield in this case was defined as the percentage of all attempts where silicon nanowire synthesis took place on the growth structure and a contact to the secondary structure was made. The latter requirement is the more challenging attribute of the process, sensitive to varying growth rates, predefined gaps between the MEMS structures and off-centered growth patterns.

A final noteworthy yet rare observation is of broken nanowires following a successful assembly process. That is, in a handful of samples, a few, short nanowires

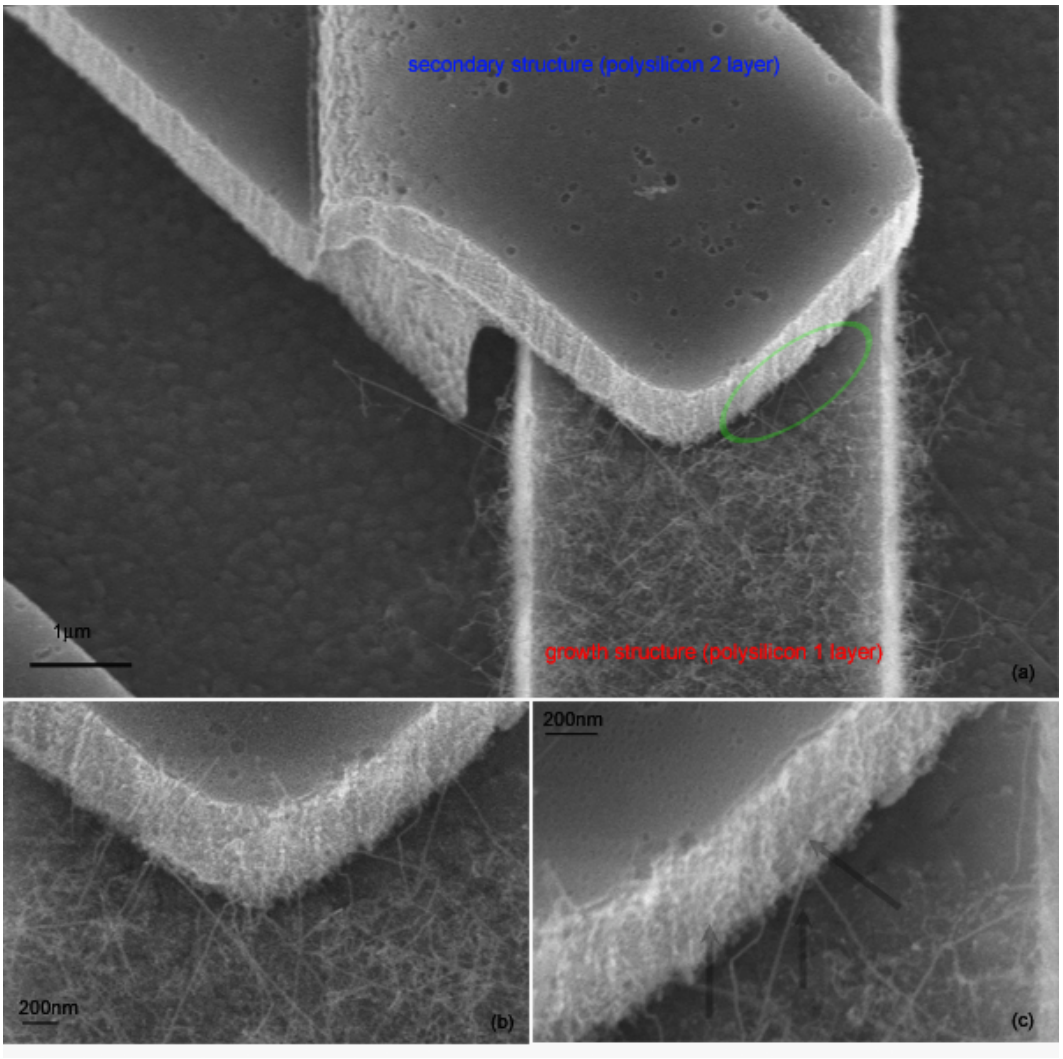

Figure 4.5. The demonstration of vertical nanowire growth to link together vertically offset polysilicon MEMS structures. (a) Localized silicon nanowire growth on a U-shaped structure overlapped by a secondary structure. The two structures are separated by a 0.75µm air gap. The close proximity of the secondary structure does alter heat dissipation regime of the growth structure. (b) & (c) nanowires growing from the surface of the growth structure transcend upwards and make contact to the secondary structure.

attached to the secondary structure are visible (Figure 4.6) indicating a failure along the nanowire's length rather than the contacts. It appears that this phenomenon has likely occurred during or just following the synthesis process. The free end of the nanowire appears to curl up upon itself. The splitting of the nanowire could possibly be attributed to the growth structure contracting upon cool down and thus tugging on

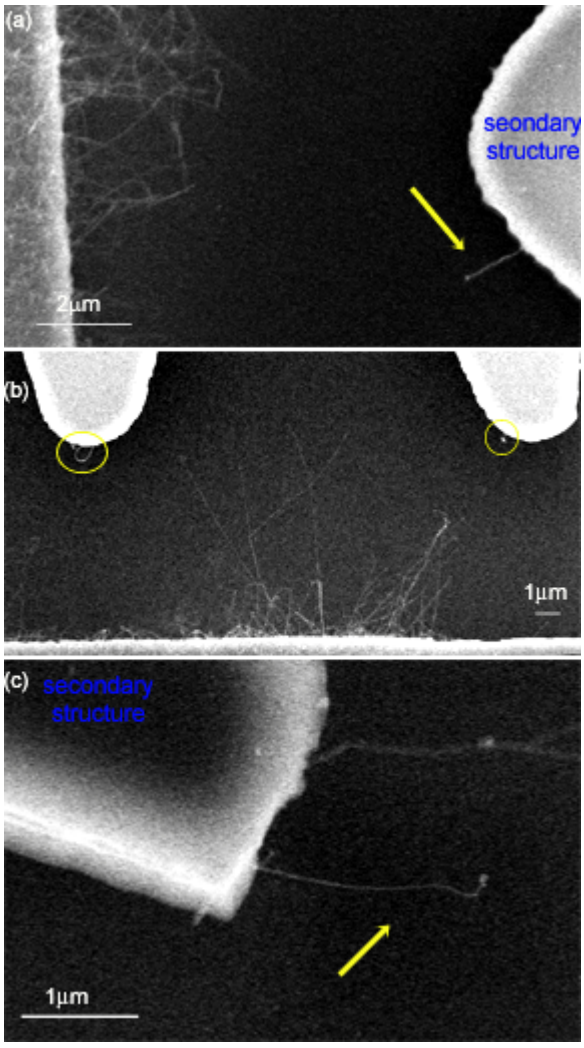

Figure 4.6. Loss of contact as nanowires fail along their length thus providing evidence that contact to the secondary structure was established. (a) The growth structure is the left structure and a single nanowire is seen to protrude from the opposite secondary structure. (b) The growth structure is the bottom structure and short nanowires extending from two opposite locations are evident. (c) The secondary structure and a broken nanowire where the point of failure is almost 2µm away from the contact location, at the secondary structure.

the nanowires. However, it is odd that this behavior is so rarely observed. It may be further attributed to the presence of defects along the nanowire's length; possibly creating weak points, or perhaps the case of a very taut nanowire with no slack to handle an additional tensile force applied upon cool down. This behavior was not found to be uniquely tied to a specific growth, or secondary structure design, or

synthesis conditions. Nonetheless, this observation serves to confirm that contact to the secondary structure is indeed established during the synthesis process.

4.4.2 Electric-Field Assisted Growth

The response of the silicon nanowires to the presence of a localized electric-field during the synthesis process is evaluated in this section. The following series of figures demonstrates experimentally that increased electric-field strength leads to improved nanowire order and organization. Figure 4.7(a) illustrates the lack of ordering and organization of the nanowire growth when no electric-field is applied between the two structures across a 5μm gap. It is also observed that many nanowires are resting on the top surface of the secondary structure (right structure). In Figure 4.7(b) a weak electric field, 1V/μm in strength, is applied between the structures, and an improved level of nanowire ordering is visible across the 5μm gap. Figure 4.7(c) shows further improved nanowire ordering and alignment as the electric-field strength is increased to 5V/μm. A comparison of Figure 4.7(b) and (c) reveals an approximately 5-fold decrease in the number of nanowires growing over and/or resting on the top surface of the secondary structure as the electric-field strength is increased from 1V/μm to 5V/μm. Instead, a large number of nanowires now make contact to the sidewalls of the secondary structure without growing over and/or resting on the top surface. The results illustrate that although the silicon nanowires are intrinsic, a response to the presence of the electric-field is discernible. It is surmised that even in the absence of a dopant source, mobile electrons should be

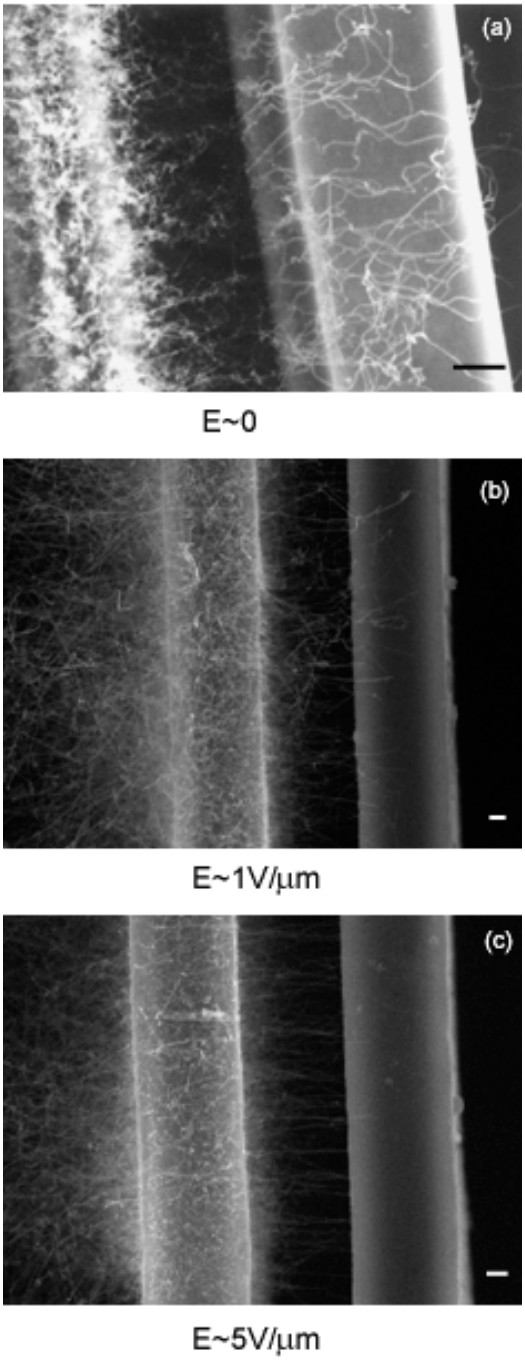

Figure 4.7. Illustration of silicon nanowires' response to the presence of an electric-field. In all cases the growth structure is on the left and the electric-field is pointing from left to right (a) No electric field applied yielding poor organization across the gap. (b) Evidence of improved SiNW organization between the MEMS structures where a light electric-field is present (E~1V/μm). (c) Further improvement in SiNW organization with increased electric-field strength (E~5V/μm). A significant decrease in the number of nanowires growing over or resting on top of the secondary structure with increased electric-field strength is noted. (All scale bars are 1μm.)

available for the interaction with the electric-field during the synthesis process, as the silicon nanowire synthesis process takes place at a local temperature of 600-700ºC which should be sufficient for the thermal excitation of electrons [67, 80]. Further, another important benefit of the presence of the electric-field is the increased probability of the nanowires contacting the sidewall. The interaction between nanowires and the secondary structure is important in assessing the quality of each contact. While a contact to the sidewall should indicate a weld-type bond [29], nanowires resting on the top surface may suggest a van der Waals interaction at best.

The role of the fringe field and field intensification is examined in Figure 4.8 for two standard U-shape structures with electric-field simulated as illustrated in Figure 4.3(a). Although the micromachining process results in rounded corners in Figure 4.8(a), the influence of the fringe field effect on the orientation of the growth of nanowires is observed as nanowires bend along fringe field directions. While the experimental setup yields a 5.2V/μm uniform field in the gap away from the corners, the electric-field strength at the corner can reach 7.5V/μm as indicated by the simulation. By comparing simulation and experimental results, the role of the electric field can be better assessed. The simulated electric-field intensification at the corner is observed as nanowires transcending the gap within 1μm away from the corner of the growth structure's are angled towards the secondary structure's corner. Nanowires growing beyond the edge of the growth structure are seen to respond to the presence of a fringe field. Nanowires longer than 3μm and within a field strength region of 2.7V/μm or greater bend along fringe electric field lines as they make

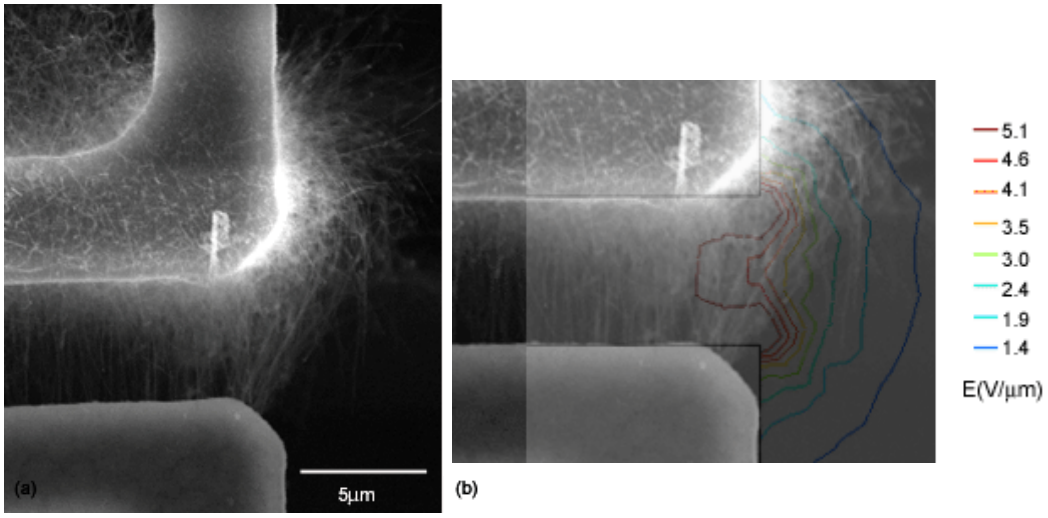

Figure 4.8. The role of a localized electric-field near a corner. (a) Silicon nanowires bending along fringe field lines as simulated in Figure 4.3. The electric field strength at the corners is 7.5 V/µm while the fringe field strength drops from ~4.1 V/µm to ~2.4V/µm within 1-2µm to the right of the structures. (b) A contour plot is superimposed over the studied growth region illustrating the diminishing electric field strength away from the structures.

contact to both MEMS structures.

It is possible to design sharp tips to serve as locations of enhanced field strength. In Figure 4.9 the tendency of the nanowires to veer towards these regions is seen. It is important to remember that the SEM images presented in this work are representative of the as synthesized status as interaction between the nanowires and the SEM's electron beam rarely occurs and only occurs under very high magnifications and after long imaging times. For the crescent shaped secondary structure described earlier, SEM images illustrate the silicon nanowires seeking the sharp tips (Figure 4.10). Experimentally, the sharp secondary structures, placed at −60V, are located 5µm away from the growth structure which is at approximately 5V at the center, yielding a calculated electric field value of 13V/µm and a peak

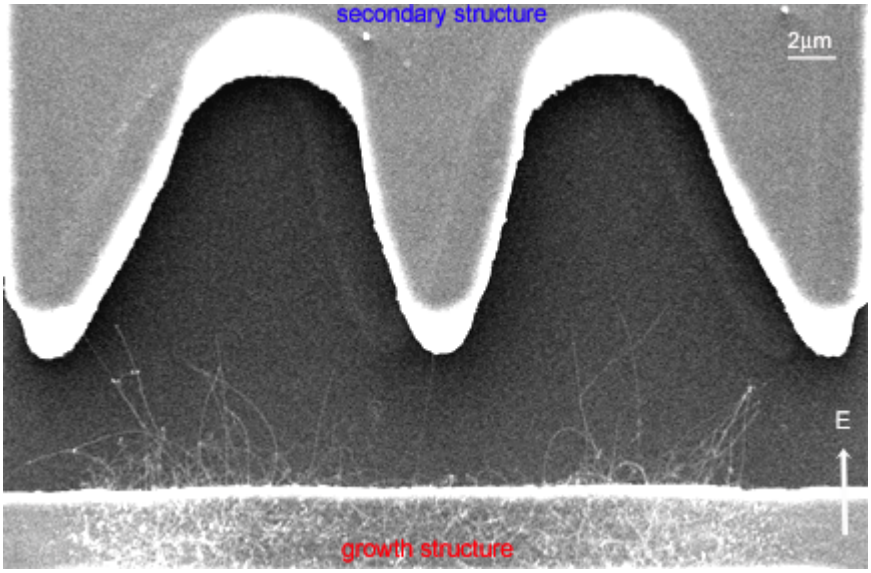

Figure 4.9. Intrinsic silicon nanowire tendency towards locations of enhanced electric-field strength. The bottom structure is the growth structure and the electric-field points upwards towards the secondary structure. The nanowires are seen to seek regions of enhanced field strength.

simulated value of approximately 30V/µm. The electric-field intensification may be actually further enhanced, in this case, as the fabrication process yields a slight overhang at the edges, truly forming a three dimensional tip, or nearly a cone which analytically corresponds to a more significant localized enhancement [79]. The electric field intensification, however, occurs locally and quickly drops in value away from the apex [79]. This effect is clearly seen as the nanowires' order and organization in regions 10-15µm away from the center of the growth structure significantly decrease. The electric-field strength in these regions is reduced to approximately 5V/µm. Based on the nanowires' behavior it is concluded that stronger fields will contribute to better nanowire alignment. Improved alignment as a function of increasing nanowire length is also evident in these experiments. As predicted [42] and illustrated in Figure 4.10, longer nanowires show better alignment

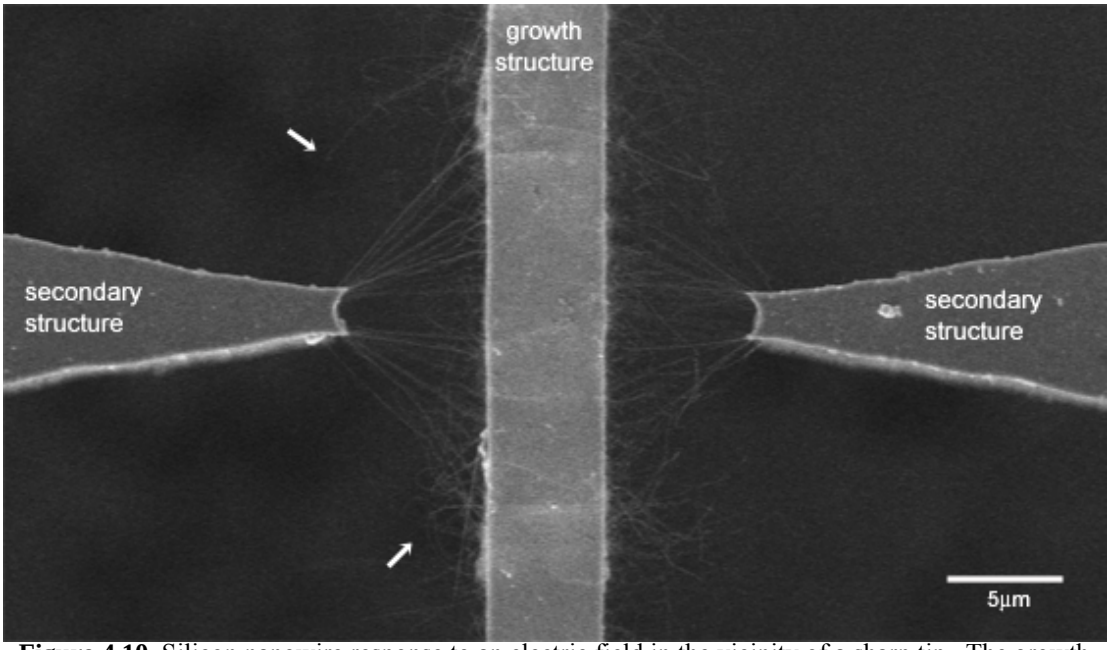

Figure 4.10. Silicon nanowire response to an electric field in the vicinity of a sharp tip. The growth structure is the center structure while double-tipped crescent shaped secondary structures are positioned 5μm away. Significantly improved nanowire organization is observed as the electric field strength amplifies to ~30V/μm at the apex of the secondary structure. With increasing distance from the tips the electric field strength decreases and the lack of organization, specifically of shorter nanowires is evident. Longer nanowires (top left), on the other hand, show a better response.

than shorter nanowires. Short nanowires, extending 2-3μm into the gap as visible in Figure 4.10, appear to stray from the induced field's direction and assume random orientations. Additional analysis in regions of reduced field strength (as discussed above) illustrate that longer nanowires (≥8μm) are indeed guided by the field.

Further evidence of the role of the electric-field can be made with respect to the nanowire attachment to the secondary structures. For example, it is observed that no two nanowires make contact to the exact location on the secondary structure (Figure 4.11). It is hypothesized that once a contact is made, the local electric charge is partially neutralized or modified and as such the local electric field strength is slightly reduced. In the case of the crescent shaped secondary structures, all contacts are

made to the regions of the sharp tips where the electric-field is strongest. In addition, the scalloped MEMS structures' sidewalls, an artifact of the bulk etching process, as seen in Figure 4.11(b), also contribute to regions of slightly stronger electric-field, and nanowire contacts seem to be made at these protruding locations.

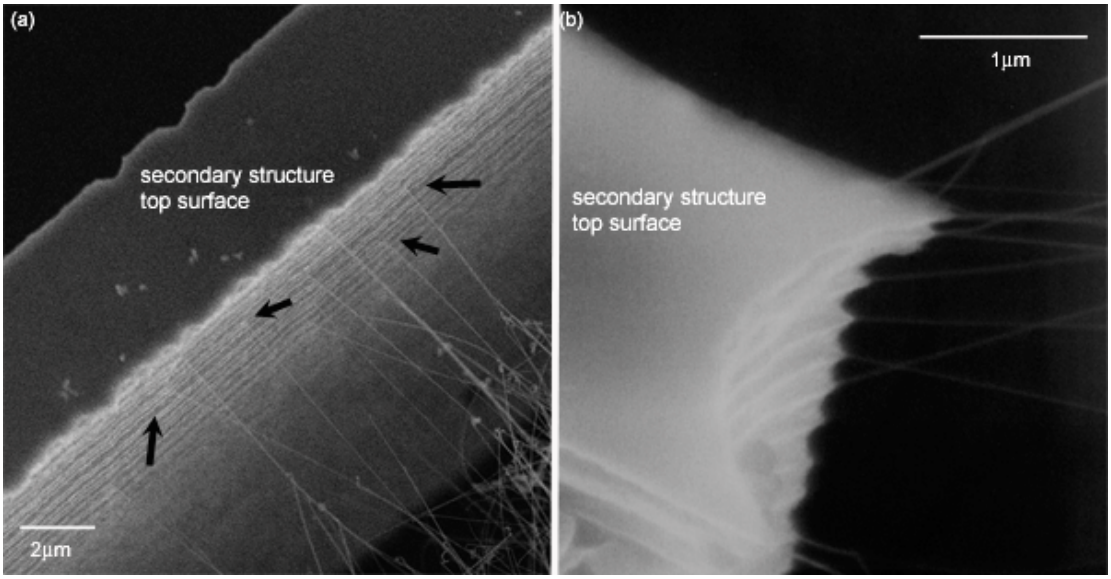

Figure 4.11. Nanowires contacting sidewalls. (a) Nanowires contacting the sidewall of the secondary structure. (b) High resolution image of the contact to the secondary structure in Figure 4.10. It is evident that the SiNW tend to contact the secondary structure away from the center region of the structure (lower electric field strength) and preferably contact the sharp edges where the electric field strength is higher. In addition, preferential contacts at protruding locations are evident.

4.5 Summary

This chapter extends the basic localized nanowire synthesis method to develop a framework required to realize a two-terminal-self-assembled micro-to-nano system. The localized process provides the advantage as the nanowire synthesis ceases once contact with the cold, secondary structure is made due to the reduction in temperature of the liquid alloy. This additional control is an improvement over current methods,

as it has been shown [29] that in a global heating environment the nanowire growth process will continue, from one surface to another, indefinitely as long as the temperature was sufficient. The synthesis time is determined by the width of the gap between the MEMS structures, or the desired length of the nanowires. Furthermore, the MEMS structures may also serve as electrodes for the application of a localized electric-field during the synthesis process. The introduction of a localized electric-field offers a simple yet reliable method for enhanced control over the placement and orientation of even intrinsic nanowires. Locally applied electric-field, 5-13V/μm in strength, appears to trigger a response from even intrinsic silicon nanowires. In addition, field enhancement effects, manipulated using the secondary structure's shape and configuration also appear to play a positive role.

5 Characterization, Post-Processing and Functionalization

5.1 Introduction

While previous chapters discuss the development of a unique approach, its basic attributes and methods to control it, here, more advanced considerations necessary to provide a better understanding of the process and more importantly enable its application in practical devices are addressed. First, transmission electron microscopy (TEM) is used to confirm the growth mechanism and provide additional information about nanowires produced in a local heating environment. Next, electrical and mechanical attributes of the self-assembled two-terminal system are considered. Finally, a proof-of-concept sensor application is introduced.

5.2 Characterization

5.2.1 Verification of Growth Mechanism

Up to this point it was assumed that the VLS process is responsible for the resulting 1-dimensional silicon nanowire growth. However, due to the unconventional approach to realizing this reaction, it was necessary to confirm that the VLS process is indeed the phenomena at hand. In order to verify the occurrence of the VLS reaction studies seeking VLS characteristics were conducted. As previously discussed, the VLS mechanism is a tip growth process uniquely

characterized by the presence of a metallic catalyst at the free tip of the silicon nanowire [7]. Identifying the presence of the metallic nanoparticle at the free end would confirm the suggested growth mechanism. TEM was required to distinguish the difference material types yet a significant obstacle to TEM analysis was the incompatibility of the sample with TEM sample requirements. TEM samples are required to be electron transparent and while the silicon nanowires are inherently electron transparent, the supporting MEMS structures and the chip are not due to their thickness.

5.2.1.1 Sample Preparation

Traditional methods of preparing substrate bound nanowires for TEM analysis require sonicating the nanowires in solution and dispensing a droplet of solution onto a TEM grid [18, 28]. This approach, however, is not a practical solution in this case, primarily due to the low nanowire count on the chip which a priori reduces the number of nanowires which may be available for the TEM sample. Overall, the main disadvantages of traditional methods include the possibility of low yield and the inability to relate growth condition to the resulting nanowires. Under traditional nanowire synthesis methods (global heating environment), the latter is not a critical issue; however, due to the temperature variation through the growth region in this process, capturing these parameters was of interest as well. Therefore, alternative approaches to TEM sample preparation were explored. With the requirement of maintaining the micro-to-nano contact, the following options were explored: using tweezers and probes to break and remove the growth structures from the chip, using a

Focused Ion Beam tool (FIB) with a gallium ion beam to cut and remove the growth region, and finally using the microfabrication process to remove selected regions of the substrate below the MEMS structures to create through-holes. All these approaches were made under the assumption that the nanowires 'hanging over' the thicker MEMS structures could be imaged while thick regions would simply appear dark.

The first approach failed since the growth structures were not designed to be easily and intentionally broken. While controllable breaking the growth structures was difficult, keeping track of the detached pieces proved impossible. The second approach failed due to heating generated by the cutting procedure. Figure 5.1 illustrates the nanowires on a growth structure cut by the FIB. It seems that high temperatures were reached in the vicinity of the growth region and the nanowires are clearly disfigured. The growth region closest to the cut location shows more significant damage. However, the cutting process clearly did not introduce temperatures near the melting point of silicon as the SCS MEMS structure remains in tact. It is reasonable to assume that the nanowire distortion is associated with melting upon reaching the eutectic temperature of the AuPd-Si system followed by solidification upon cool down. The feature size at the 'tips' is visually larger than feature size at the base.

The third approach proved most suitable. The process required an additional lithography step to define the backside holes and a long anisotropic silicon etch to remove the sections of the substrate. Following the localized synthesis process, the

MEMS structure-bound nanowires are hanging over an empty space. In addition, the die size was designed to fit within a standard TEM sample holder 3mm in diameter. This process, thus, guarantees a TEM compatible sample once the synthesis process is completed, and greatly simplifies the sample preparation process.

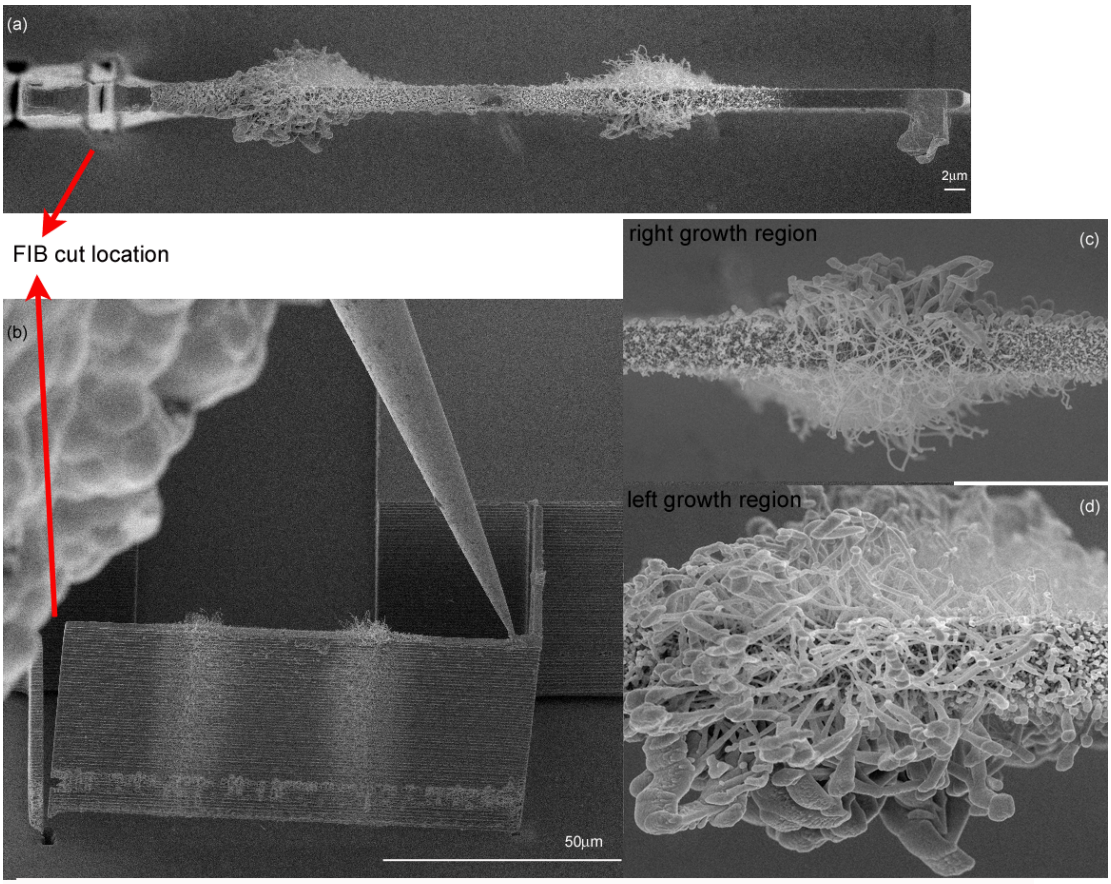

Figure 5.1. An attempt at TEM sample preparation. (a) A top view of a MEMS structure and silicon nanowire growth after an attempt to detach the growth structure from the chip. (b) A side view of the 200μm long, 2μm wide and 50μm thick SCS MEMS structure, the FIB cut and a probe welded to the structure to secure the structure. (c-d) A high resolution image of the right and left growth regions illustrating substantial disfiguring and melting of the nanowires as a result of the heating produced during the cutting process.

5.2.1.2 TEM Analysis

TEM images seen in Figure 5.2 assist in confirming the VLS growth mechanism

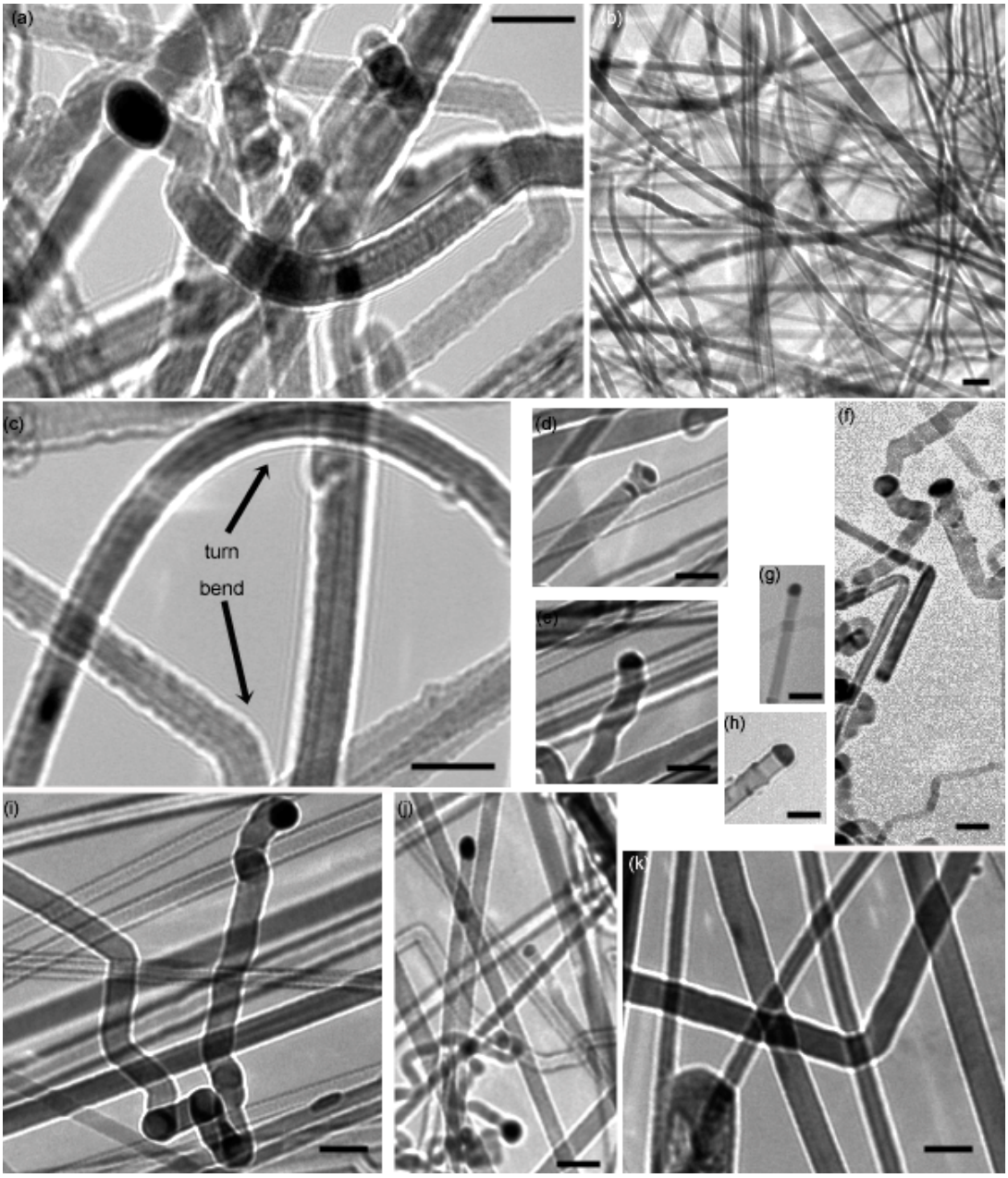

Figure 5.2. TEM images of localized silicon nanowire synthesis. (a) A 30nm in diameter nanowire with a slightly larger catalyst clearly seen at the tip. (b) A high density region of suspended nanowires. (c) Nanowires showing high flexibility as they smoothly turn about while others make very sharp turns. (d) A 75nm diameter nanowire with a smaller catalyst at the tip - a non standard result; possibly due to partial metal precipitation from the catalyst prematurely as seen by the dark strip just below the tip. (e) A well formed silicon nanowire-catalyst interface. (f) Kinking and twisting nanowires as well as nanowires bending at sharp angles. (g-h) Well formed nanowire-catalyst interfaces. (i) Significant kinking and orientation change towards the end of a 75nm diameter nanowire. Straighter nanowires are seen in the background. (j-k) Unbent, kinked, and sharply bent nanowires. (All scale bars are 100nm.)

as specifically illustrated by the tip growth phenomena. Metallic nanoparticles at the free end of the nanowires are visible as the contrast (the nanowires are light and the tips are dark) suggests the presence of a different, heavier element. The TEM analysis also indicates that the nanowires are single crystal silicon nanowires with a significant amount of defects present. Although only a few samples were studied using TEM capabilities, it is expected that the TEM samples are representative of all synthesized samples. During the TEM analysis, the nanowires were observed to move around as a result of interaction with the electron beam. Since the nanowires occupy a wide range of vertical space, the images are taken such that a portion of the nanowires is in focus while others at different focal planes are not. The TEM images also provide an improved measure of nanowire diameter, catalyst dimensions, bending angles of the nanowires and visualization of nanowire growth tendencies at process termination.

The average nanowire diameter for the TEM samples was determined to be 45nm with a standard deviation of 21nm for a collection of just over 100 nanowires studied. A minimum diameter of 9nm and a maximum diameter of 102nm were measured (Figure 5.3). A ±5nm error is associated with these measurements. The wide distribution of nanoparticle size and therefore nanowire diameter is an indication of the randomness associated with the breakdown of the thin film catalyst layer. This fact along with the wide temperature range over which the diameter measurements were conducted account for the large standard deviation associated with this analysis. It is important to note that the TEM analysis of these samples did not permit

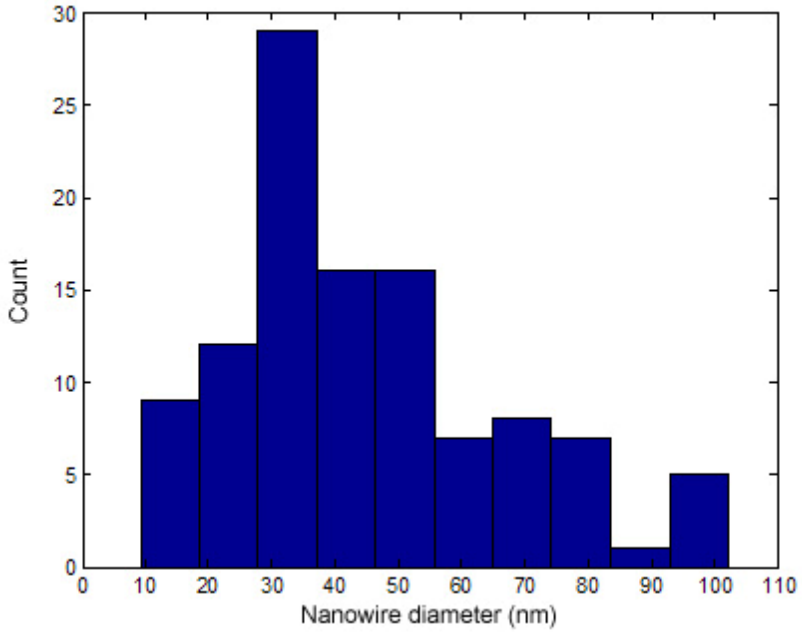

Figure 5.3. Statistical nanowire diameter distribution based on TEM assisted diameter measurements. The average nanowire diameter is 44.8nm with a standard deviation of 21nm for the 110 nanowires studied.

distinguishing the native oxide layer from the bulk of the silicon nanowires, and therefore all diameter measurements include the native oxide layer. Based on the literature, the thickness of the oxide layer is estimated to be 1-3nm thick [30]. The initial nanoparticle size, resulting from the breakdown of the thin catalyst film can be estimated to range between 7nm and 65nm based on the documented relationship between nanoparticle size and nanowire diameter (Figure 2.2 although this relation is based on a gold-silicon system). Experimental and analytical results presented in the literature suggest that the final nanoparticle, or solidified liquid alloy, dimensions may be equal or slightly larger than the nanowire diameter [9, 12, 30]. Often a flat interface between the nanowire and the nanoparticle is noted, and the nanoparticle takes a spherical or hemispherical shape (Figure 5.2(a, e, g, h)). For the nanowires

studied in this work, this relation holds in 75% of the cases. Deviation from this phenomenon is coupled with additional irregularities as seen in Figure 5.2(d), for example, where the dark strip below the free tip of the nanowire may indicate that a portion of the metallic catalyst has become separated from the whole yielding an abnormally small catalyst at the tip. In addition, oxidation of the nanowire also contributes to deviation from the expected relation. In estimating the final diameter of the nanoparticles from the TEM images, it appears that one can measure a major and a minor axis length where the major and minor axis dimensions account for the non-spherical shape of the nanoparticle. The relationship between nanowire and nanoparticle diameter is seen in Figure 5.4 with respect to the initial (extrapolated) and final nanoparticle diameter (only major axis dimension is plotted). The initial nanoparticle diameter (green line) is extrapolated based on the relationship in Figure 2.2, and a 1-to-1 nanowire-to-nanoparticle relationship (dark line) is plotted as well. This plot further suggests that the final nanoparticle dimension is on average approximately 4nm larger than a nanowire synthesized below it. The composition of the initial and the final catalyst has not been studied in detail as EDX (energy dispersive x-ray) attempts did not provide the required resolution. However, based on the literature it appears that the palladium content may be minimal [69, 70, 81]. Observation of the nanowires' cross-section over their length generally indicates a uniform cross-section and thus a constant diameter. Rarely does a decrease in diameter from base to tip is noted probably since the synthesis conditions do not support non catalyzed silicon deposition. While some nanowires exhibit no bending

or kinking, others exhibit a single bend or reorientation event while yet another portion of the nanowires exhibits multiple kinking and bending events (Figure 5.2(c, i, k)). The flexibility of the nanowires is also evident as nanowires are clearly seen to

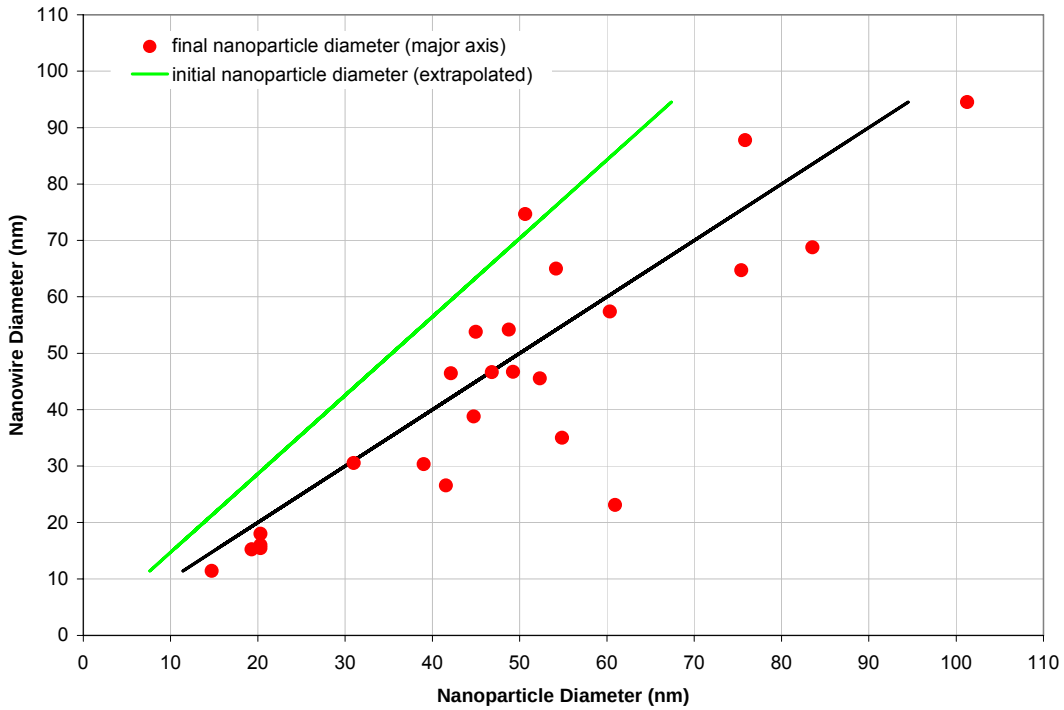

Figure 5.4. Nanowire-nanoparticle diameter relationship. The final nanowire diameter is generally smaller or equal to the final nanoparticle diameter unless irregularities occur during the growth process. The initial nanoparticle diameter (green line), extrapolated from the data in Figure 2.2, as well as a 1:1 nanowire: nanoparticle relationship are displayed.

smoothly turn (Figure 5.2(c)). The agility of the nanowires can be further appreciated by considering the path they generally transcend in this work; from the top surface of the growth structure to the sidewall of the secondary structure. On the other hand, sharp bending angles ranging from 90º to 160º are also measured. While bend angles of 55º or 90º may indicate a change in growth orientation, other bend angles may be more difficult to explain. It has been suggested that 'gradual bending' is induced by elastic strains [10]. Alternatively, bending and kinking may be attributed to non-ideal

synthesis condition as well as significant changes in growth conditions which introduce instabilities at the liquid alloy-silicon nanowire interface during the growth process [6, 23]. The experimental setup introduces sources of instability including the termination of the gas flow and the temperature drop as the power supply to the growth structure is cut off. A correlation between abrupt changes in temperature during whisker growth and kinking behavior has been reported in [82]. More specifically, it is suggested that unidirectional growth requires an isothermal environment and that a sudden increase or decrease in temperature introduces instabilities that can be compensated for by the growth process. An abrupt decrease in temperature may be analogous to the final growth conditions present in this work. The change in temperature appears to coincide with a reduction in the liquid alloy's volume which requires rapid precipitation of excess silicon and thus an increased growth rate to enable a return to equilibrium conditions. The increased growth rate may explain the kinking behavior near the tip. Along the same lines, the use of SiH_4 has been linked to poorer quality nanowires possibly due to rapid decomposition rate and thus high rate of silicon impingement upon the liquid alloy while improved quality has been shown with $SiCl_4$, a more stable vapor phase [83]. The varying nanowire behavior, within the same growth region is somewhat puzzling however. In this work bending and kinking events appear to take place under seemingly constant growth conditions, while subject to changing conditions and somewhat randomly, as for example, one nanowire appears to be of good quality while a neighboring nanowire displays much bending and kinking. Therefore, it is hypothesized that in

this case, the interactions among the nanowires during the synthesis process along with process instabilities and the consequences of using SiH_4 contribute to these events.

Re-evaluating the conditions at the nanowires' tips based on Figure 4.11 and the TEM analysis where a secondary contact is established, these contacts appear clean and the kinking and bending, which are prevalent with the free nanowires (Figure 3.7(g)), are visually minimized. It is expected that the temperature at the tip of a nanowire drops to room temperature immediately, once it is in contact with the cold secondary structure as the cold structure contributes to improved heat dissipation rates. On the other hand, it may take slightly longer for the hot nanowires suspended in vacuum to drop to a low temperature when the power is turned off depending on the thermal capacity of the MEMS structure. In the latter case, the VLS reaction may still be taking place while subject to changing thermal conditions yielding

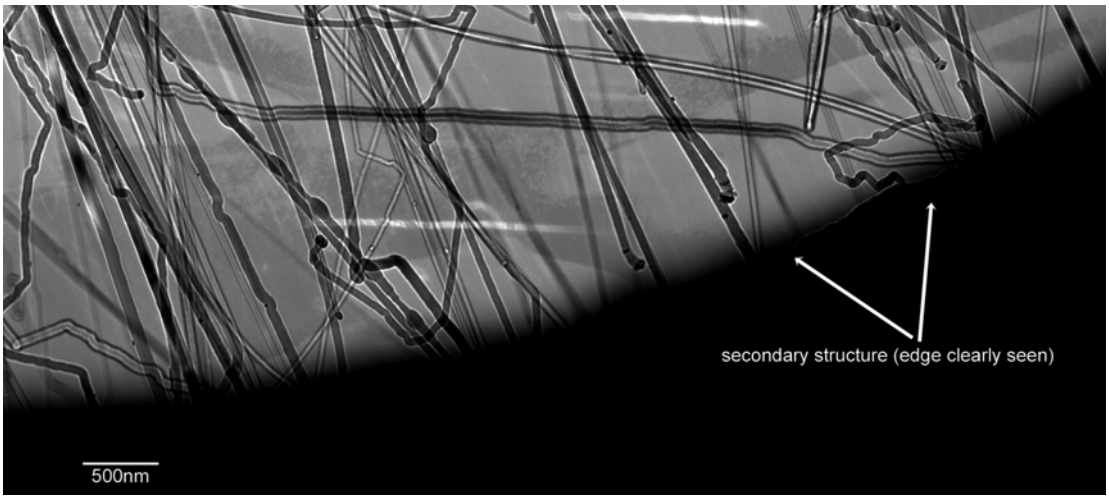

Figure 5.5. TEM imaging near edge of secondary structure. A micron long region clearly displays the edge with no shadowing. The level of kinking, bending and twisting near the tip appears to be reduced for nanowires contacting the secondary structure.

irregularities near the free ends. TEM analysis of nanowires contacting the secondary structure do not illustrate a change in contrast near the end of the nanowire which could serve as an indication that the liquid alloy has become a part of the bulk structure upon contact thus forming a robust mechanical bond (Figure 5.5). At the same time, it is worth noting that the sample configuration does hinder the quality of these observations due to shadowing caused by the bulk structure and wide focal depth of the nanowires.

5.2.2 Electrical Characterization

Evaluating the electrical properties of the self-assembled system and particularly the micro-to-nano contact has proven to be a rather challenging task. Electrical characterization of the system was performed using an Agilent 4156 parameter analyzer capable of pico Amperes of resolution. These measurements were conducted from a bond pad of the growth structure through the nanowire array to a bond pad of the secondary structure as seen in Figure 5.6. Since the as-synthesized silicon nanowires have a very low carrier concentration, the system's response is very

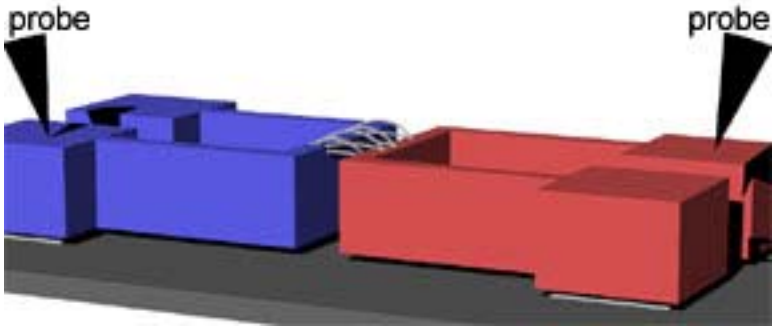

Figure 5.6. Experimental setup for I-V characterization of self-assembled system. A contact to the anchors of both the growth and secondary structure is made. Voltage is swept on the growth structure and current is measured at the secondary structure.

close to typical noise levels (tenths of picoAmps), and its performance may be impacted by the surroundings. In addition, the low carrier concentration in the nanowires and the contact with the heavily doped MEMS structures likely lead to a barrier and a non-ohmic contact.

The current-voltage characteristics of the devices are indicative of low carrier concentration as illustrated by the low current levels while the non-linearity in the curve points to the presence of non-ohmic contacts. Figure 5.7 illustrates non-linear current-voltage relationships as only pico Amps of current pass through the system even when 10V are applied across the system. However, due to the high resistance of the nanowires, low current values are expected. Theoretical calculations assuming the resistivity of intrinsic silicon ($3x10^5$ ohm-cm) and using typical nanowire dimensions, 50nm in diameter and 5μm in length, are in agreement with experimentally observed values and yield a resistance of $7x10^{12}$ohm per nanowire. To verify that the measurements are indeed representative of the current through the system, measurements were also taken prior to the synthesis process to establish a base line reading. The *Iin* and *Iout* curves in Figure 5.7 refer to the drive and sense current values respectively and serve as an indication that transport does occur through the system and is not lost to the surroundings. In addition, the number of observable contacts does seem to be related to the current carrying capacity of the system. As illustrated in Figure 5.8, increased current values are associated with an increase in the number of contacts. The I-V measurements were repeated multiple times to confirm the reproducibility of the characteristics. I-V plots sweeping

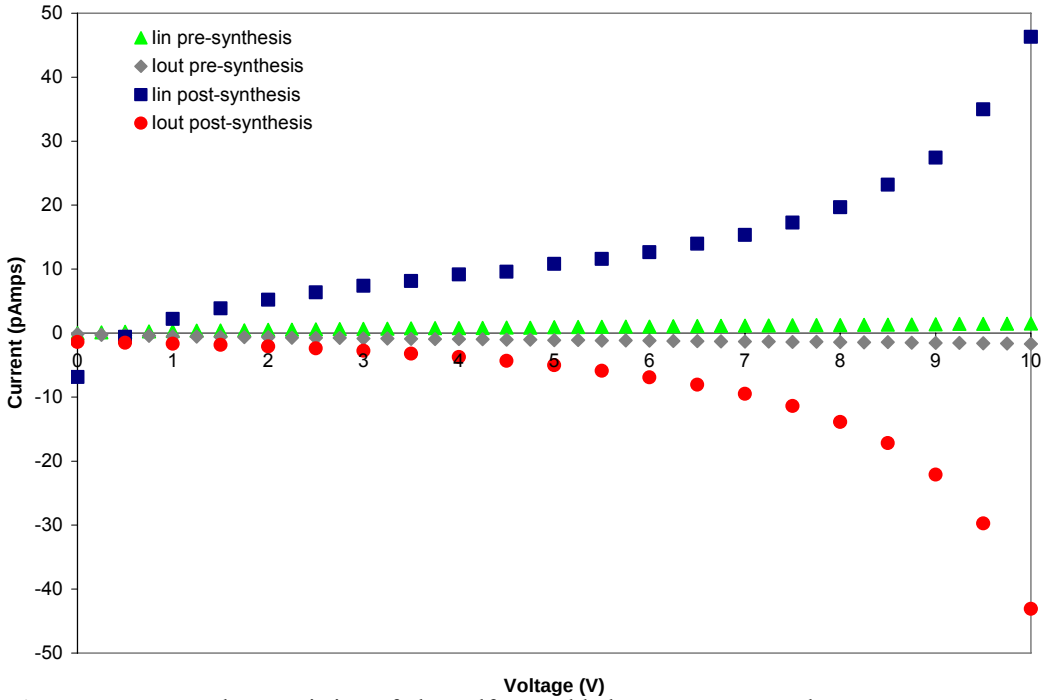

Figure 5.7. I-V characteristics of the self-assembled system. *Iin* and *Iout* represent current measurements at the growth and secondary structures respectively. The pre-synthesis measurement helps in establishing the cleanliness of the sample as well as assessing background noise levels. The non-linearly of the post-synthesis curve suggests the presence of high contact resistances.

through negative and positive voltages are bipolar and do not show evidence of rectifying behavior (illustrated in upcoming sections). When recording and evaluating the I-V data, one important issue must be considered, namely, the cleanliness of the sample. Debris or other foreign contaminants may offer a preferential conduction path to the nanowires, which could be expressed in the form of improved current carrying capabilities. It is important to inspect the chip and specifically regions near the MEMS structures when abnormally high current values are obtained.

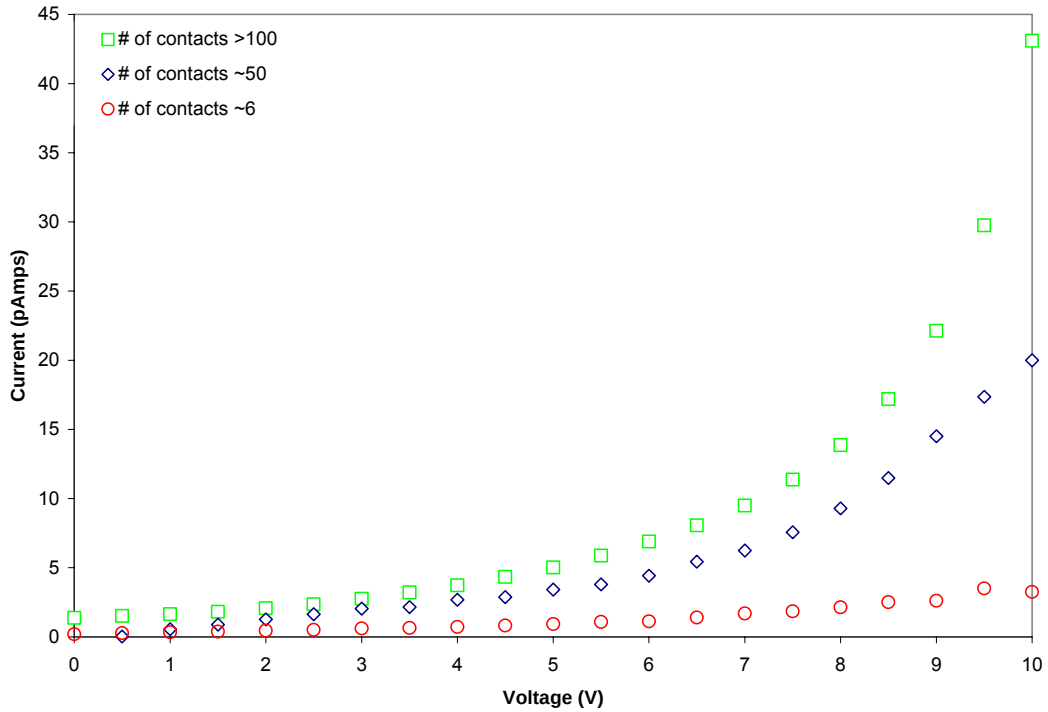

Figure 5.8. I-V characteristics of the self-assembled system as a function of observed number of contacts. It appears that as the number of contacts increases so does the current carrying capacity of the system.

5.2.2.1 Contact Resistance

While the synthesis parameters and nanowire dimension are responsible for high resistances, contact resistance presents another challenge when evaluating the properties of the system. In fact, the nature of contact resistances, specifically in conjunction with lightly doped or undoped nanowires is poorly understood [37, 84]. Although, a metal-semiconductor contact is usually considered when determining the electrical properties of a contact, the analysis presented here addresses a contact formed between highly doped silicon, close to the metallic limit and undoped silicon. In order to understand the properties of these contacts, all of the assembled system's attributes must be considered. Since the Fermi level of these two members is

different, a barrier is expected. Further, a native oxide layer, although thin, is present on the MEMS structures. It is presumed that electrons should be able to tunnel through this layer [73]. Another consideration is the fact that the assembly method presented here is not symmetric. In other words, the method by which the contact to the growth structure is established is different from the mechanism responsible for the nanowire-to-secondary structure contact. The initial contact is a solid to solid contact while the secondary contact is a liquid to solid contact. When post-synthesis methods (EBL) are used to establish electrical contacts to nanowires, maximizing the contact area is advantageous as the resistance is inversely proportional to area. However, in this case, as illustrated in Figure 5.9, the contact area is determined by the diameter of the nanowire and hence is considerably smaller than traditionally assembled devices.

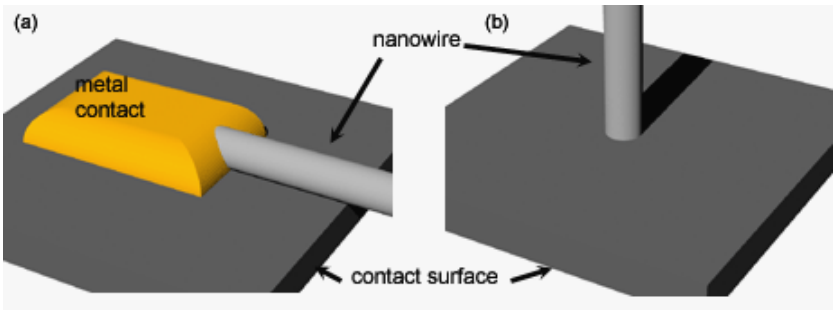

Figure 5.9. Schematic illustration of a traditional metallized contact versus a self-assembled micro-to-nano contact. (a) A high contact area contact established using EBL-based post-processing techniques and (b) a reduced contact area self-assembled contact established in-situ.

Based on the nanowire diameter statistics, the average contact area is determined to be $1.59 \times 10^{-3} \mu m^2$, while an EBL-based metal contact for a similar nanowire and a 2μm-long overlap is likely to have a contact area 57 times larger. Moreover, the literature suggests that the actual contact area is smaller than the apparent contact area due to surface irregularities, cleanliness, and interface characteristics [73]. Ideally,

the contact to the growth structure could be epitaxial in nature [22, 31]; however the presence of the native oxide may prohibit the epitaxy from taking place. Since the secondary contact is generally formed at the rough MEMS structure's side wall, the presence of the liquid alloy may favorably contribute to increased contact area.

Resistance measurements must account for both the contact resistances and the resistance of the individual nanowires. Equation 5-1 presents the elements contributing to the total resistance (R_T) across one nanowire connected at both ends to the MEMS structures using the self-assembly approach presented in this work. The terms $R_{Cgrowth}$ and R_{C2nd} refer to the contact resistances to growth and secondary structures respectively while the resistance of the nanowire is accounted for by the third term, where ρ is the resistivity of silicon (as a function of doping level), L is the length of the nanowire and r is the radius of the nanowire. Due to the variations in nanowire geometry, both the contact resistances and nanowire resistance may differ for each nanowire. While the nanowire diameter would more significantly contribute to variations in resistance, the variations in the length of the nanowires may also be significant especially when the geometry of the secondary structure presents different path lengths for the nanowires depending on the nanowire's point of origin (Figure 4.9). It is therefore best to first consider each nanowire individually and then consider all the nanowires as resistors in parallel. Although not experimentally practical, Equation 5-2 presents the total resistance in a system.

$$R_T = R_{Cgrowth} + R_{C2nd} + \frac{\rho L}{\pi r^2} \qquad \text{Equation 5-1}$$

$$R_{Total} = \left(\sum_{i=1}^{Nnanowires} \left[\frac{1}{R_{Ti}} \right] \right)^{-1} \qquad \text{Equation 5-2}$$

Finally, since the contact resistance is strongly dependent on nanowire diameter and properties of the micro-to-nano interface, it is reasonable to conclude that no two nanowires could exhibit identical properties. Beyond the physical attributes of the contacts, another phenomena dealing with the motion of charged carriers from a three dimensional bulk structure to a 1-dimensional nanostructure (although not addressed here) may also alter electrical properties.

As commonly practiced when improving microscale contacts, an anneal step has been shown to reduce nanoscale contact resistance in traditionally made contacts [2]. Here, the I-V characteristics were measured before and after a short anneal. The annealing processes included a traditional post-synthesis anneal, in a furnace environment in N_2 ambient, as well as post-synthesis localized heating of both the growth and secondary structure in N_2 ambient. Since the growth structure-to-nanowire contact is essentially being annealed during the synthesis process, in-situ annealing was also attempted by locally heating the secondary structure during synthesis. The heating level in this case must be carefully controlled as it was sought to suppress the VLS process. Disappointingly, none of the annealing attempts showed improved I-V characteristics. Ideally, the initial contact should be well annealed, following the high temperature synthesis process and only the secondary contact may require annealing. In another attempt to improve the I-V characteristics of the system, both contacts to the MEMS structures were reinforced using platinum

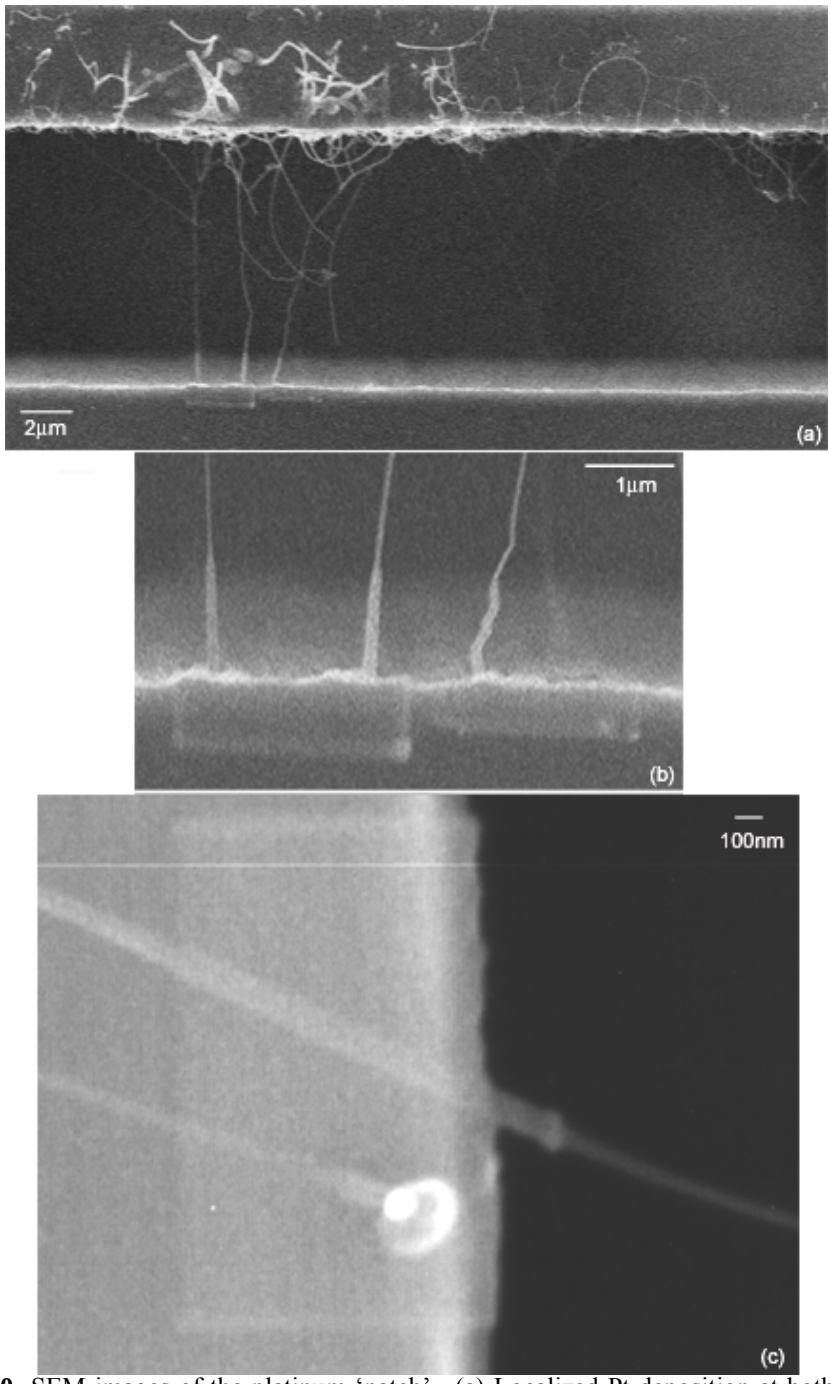

Figure 5.10. SEM images of the platinum 'patch'. (a) Localized Pt deposition at both the growth (top) and secondary structures contact locations. Since in this case the origin of the contact on the growth structure is difficult to identify, the deposition region extends through the width of the MEMS structure (the deposition region is defined by larger feature size on the surface), while at the secondary structure the deposition is further localized as seen in (b). (b) & (c) Slightly raised regions define the extent of the localized Pt deposition on a secondary and growth structures respectively. An increase in the nanowire diameter is seen as well and illustrates that the deposition region extends slightly into the gap.

deposition. Approximately 20-40nm of platinum was deposited locally using in-situ SEM deposition tool. The localization of the Pt deposition was verified using an EDX tool as seen in Appendix 9.3 to ensure that conduction does not take place through the Pt layer. Figure 5.10 illustrates the localized Pt deposition; on the MEMS structure's surface, a slightly raised region defines the extent of the Pt deposition and a nanowire, approximately 90nm in diameter, is seen to increase in size within the Pt deposition region. In the particular case illustrated by the I-V curve in Figure 5.11,

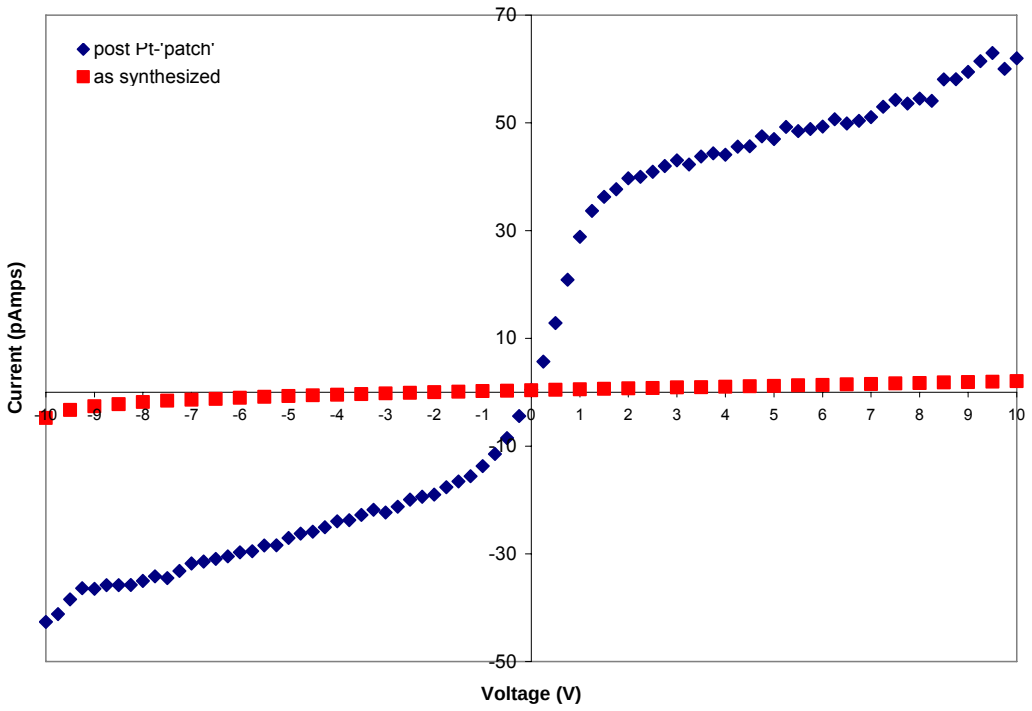

Figure 5.11. I-V characteristics before and after the application of the Pt 'patch'. The addition of the Pt 'patch' appears to improve conductivity across the self-assembled system. The non-linear behavior is still present and the curve is bipolar.

the electrical characteristics show a better than an order of magnitude improvement in the current carrying capacity of the nanowires following the application of the Pt 'patch' at the ends of two nanowires. The I-V curve, nonetheless, exhibits a non-

linear behavior indicating that non-ideal contacts as well as a rather symmetric barrier at approximately 1V are still present in the system.

5.2.3 Mechanical Characterization

Characterization of mechanical properties on the nanoscale is a rather new area of research. Currently, very few tools that enable such studies are widely available. The development of the tools and the techniques for mechanical characterization is an essential step towards developing and maturing nanotechnology. However, the behavior of the nanowires, in the context of the self-assembled system does provide some indication of mechanical response, behavior and strength.

An indication of the robustness of the integrated system may be visually recognized as illustrated in Figure 5.12, where the nanowires can easily support silicon debris that has come to rest in the gap and lies across numerous nanowires. The contact to both MEMS structures still appears in tact.

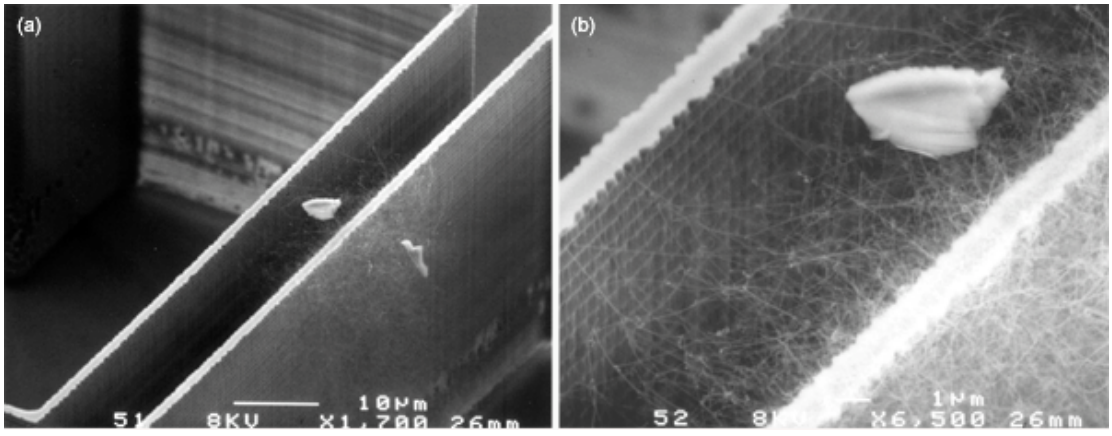

Figure 5.12. Visual illustration of the mechanical resilience of the self-assembled system. (a) An approximately 3µm-long piece of silicon debris resting upon multiple nanowires linking together two MEMS structures across a 10µm gap and (b) a close up view. The growth structure is on the right.

Another mechanical property becomes evident as a result of system functionalization attempts. Functionalization for biological sensing applications typically requires a wet processing step to place specific markers onto the sensing surface [35, 36]. As such, it was interesting to study the response of the self-assembled system to an aqueous environment. This experiment involved covering the chip's surface with a few milliliters of a low surface tension liquid, isopropyl alcohol (IPA), and allowing the surface to dry, in air, inside a 90^{o}C oven. Since it was expected that surface tension effects would play a role, an identical exposure to a liquid environment, followed by a critical point drying (CPD) step was conducted as well. The CPD process is designed to permit the phase change from liquid to vapor without crossing the liquid-vapor phase boundary and hence eliminating surface tension effects. Figures 5.13 and 5.14 illustrate the wet post processing step followed by air drying and the CPD step, respectively. In the case of the evaporation of the liquid from the surface in air, it appears that surface tension forces contribute to the loss of the secondary contact. However, as indicated in Figure 5.14, the loss of contact can be avoided by following the wet processing with a CPD process. A visual indication of the presence of surface tension effects is illustrated in Figure 5.13 as nanowires are slumping over the growth structure. These results suggest that the loss of contacts does occur during the drying processes and that the system does retain its as-synthesized configuration upon contact with the liquid phase. This experiment further suggests that the initial contact to the growth structure is mechanically stronger than the contact to the secondary structure. Finally, this experiment confirms

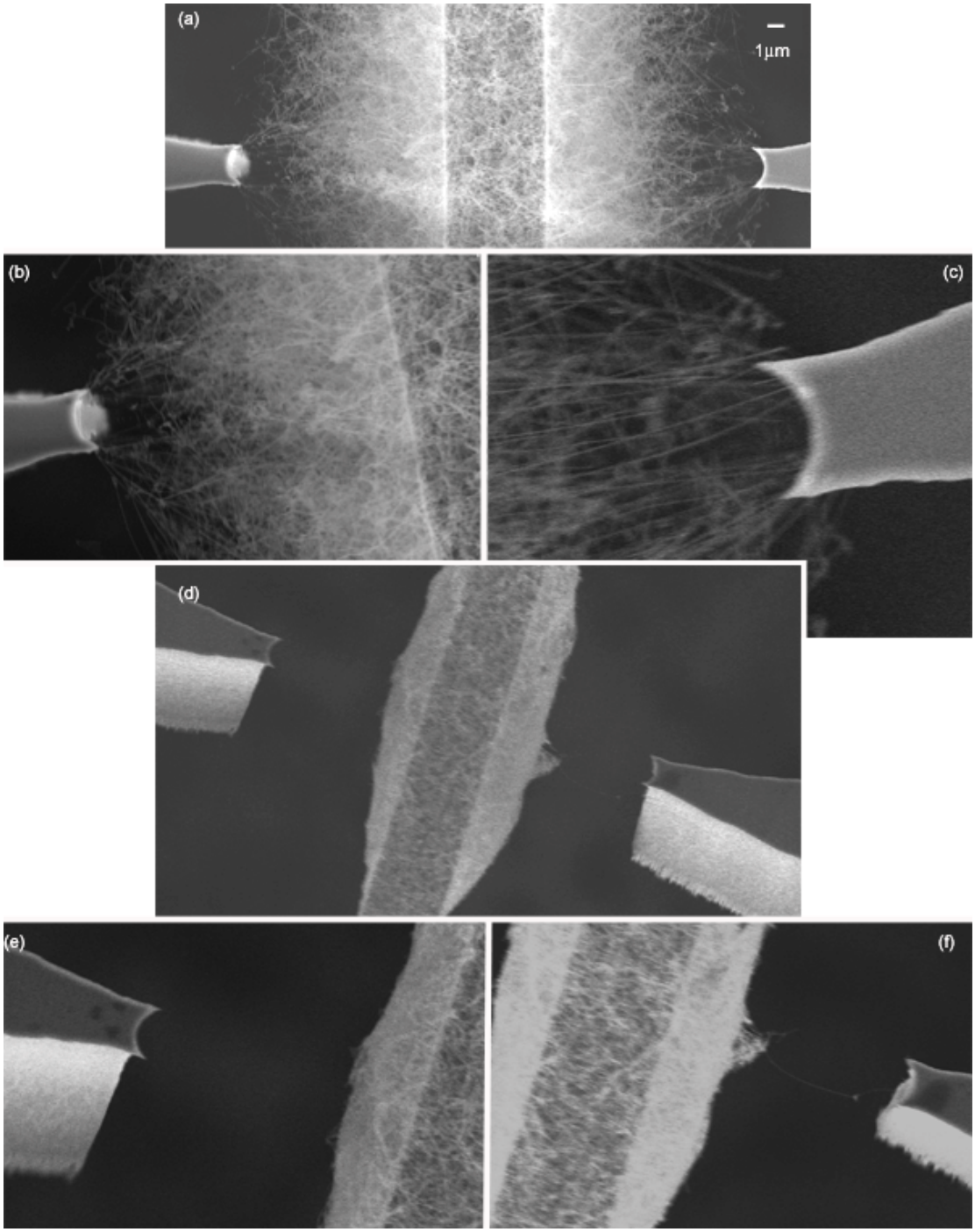

Figure 5.13. Surface tension effects plaguing the self-assembled system. (a-c) As synthesized self-assembled system (growth structure is at the center). (d-f) System after placement in a liquid environment and drying in air. Contacts to the secondary structure are lost and the nanowires are seen to slump over the growth structure.

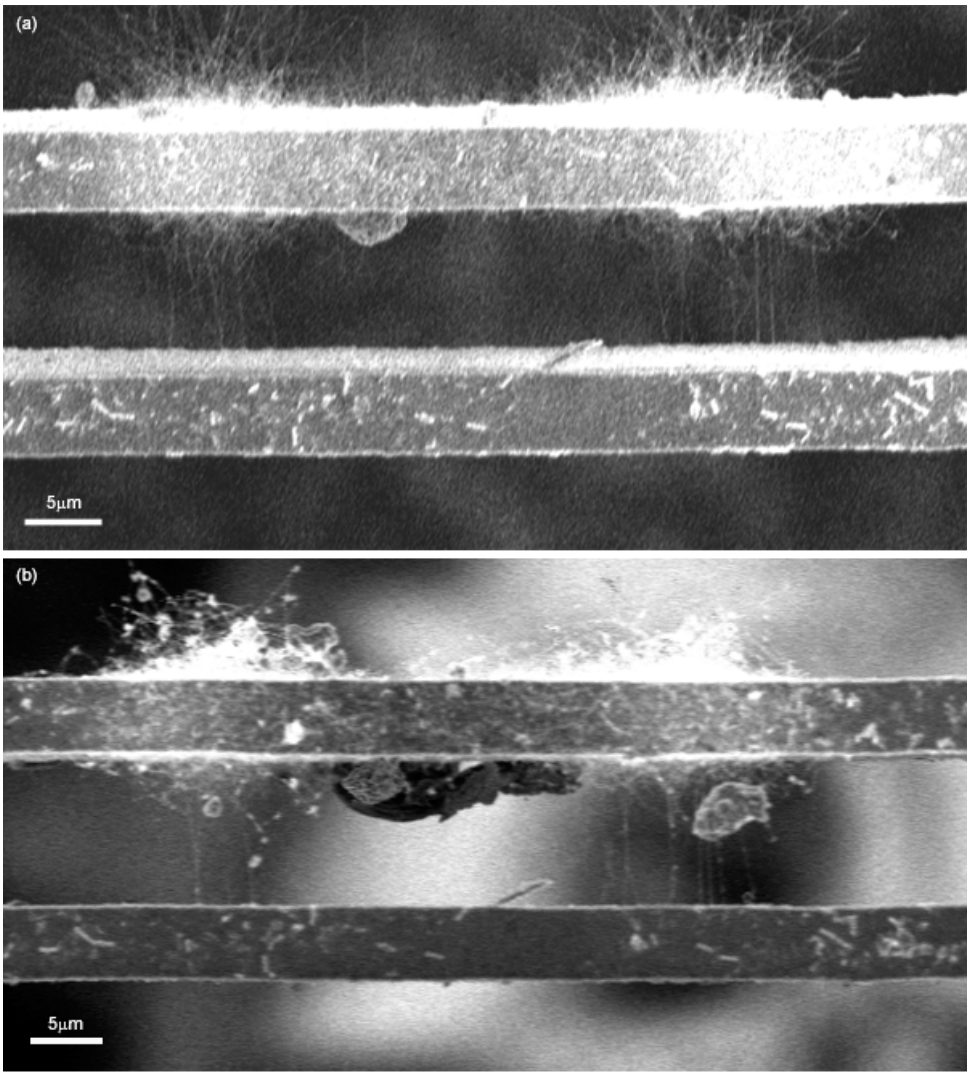

Figure 5.14. Conservation of contacts following a critical point drying (CPD) step. (a) As synthesized self-assembled system and (b) system following a CPD step. The contacts to the secondary structure are maintained. Additional debris was introduced during the CPD process, but does not appear to hinder the contacts.

that surface tension forces that are known to play a significant role on the microscale are prevalent on the nanoscale as well.

As previously discussed, the initial and the secondary contacts are formed under different conditions. While the initial contact is essentially a silicon to silicon contact, the secondary contact also incorporates the metallic catalyst. While the literature

presents some evidence that the metallic catalyst tends to spread upon contact [29], the results in this work indicate a clean contact to the best resolution afforded by the SEM, as seen in Figure 5.15 as well as Figure 4.11. This aforementioned effect with respect to the experimental setup used in this work may be minimized since the secondary contact is made to a cold structure.

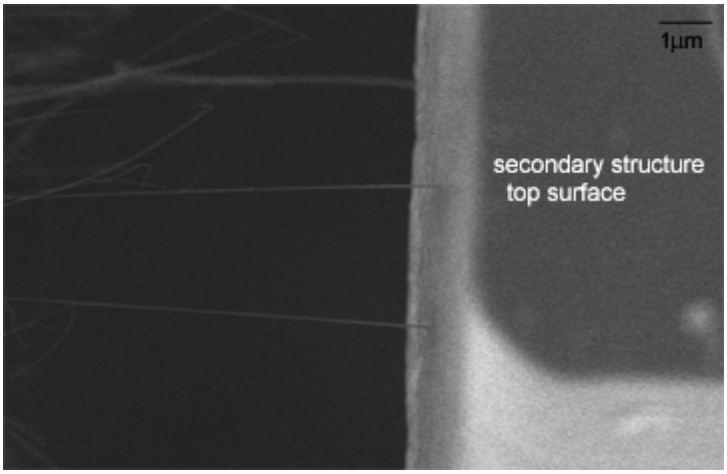

Figure 5.15. High resolution image of nanowire contact to sidewall of the secondary structure. A clean contact is evident.

The Zyvex S100 in-situ SEM nanomanipulator can be used to provide additional qualitative information about mechanical properties of the system. More specifically, the system allows interaction with individual nanowires using tungsten probes with very fine tips. While force feedback capabilities are not available with this system, a visual response does provide some information. With a single nanowire attached to probe tip, it appears, for example, that the force required to break the contact to the growth structure is greater than that required to break a contact to the secondary structure. The series of images in Figure 5.16 provides additional information about

the nanowire and the nanowire-secondary structure contact at the sidewall. In Figure 5.16(a-i) a probe is used to apply a compressive force onto a 2.4μm long nanowire. The nanowire appears to buckle and shows a maximum displacement of approximately 0.5μm when subjected to the compressive loading. The deformed

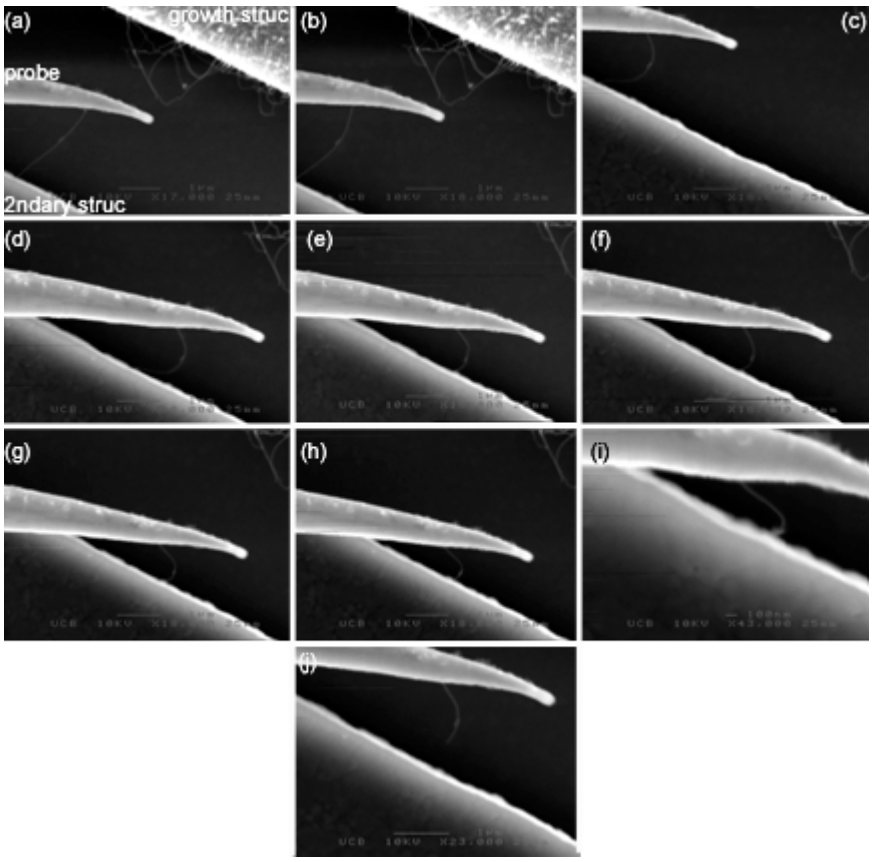

Figure 5.16. In-situ SEM manipulation of a single nanowire contacting the secondary structure. (a-i) Sequence of events depicting contacting a nanowire with a tungsten probe and slowly applying a downward buckling load. (j) The nanowire is separated from the secondary structure only when an upward force is applied. The resulting nanowire is shorter than the nanowire in (a) suggesting that the nanowire did not break at the contact with the secondary structure but rather along the nanowire.

nanowire may be partially restored to its original shape upon the application of a weak tensile force and as seen in Figure 5.16(j) finally breaks when a stronger upwards force is applied. Since the nanowire attached to the probe tip in Figure

5.16(j) is approximately 1μm long and thus shorter than the original nanowire, there is an indication that the nanowire did not break at the micro-to-nano contact but rather along the nanowire, possibly at the defect location.

5.3 Doping Efforts

The doping of silicon as well as other semiconductors is a relatively standard process. As the literature suggests, the introduction of a dopant source into the nanowire synthesis environment during the VLS process is a suitable approach for achieving reasonable doping levels. The ability to controllably and effectively dope the semiconducting nanowires studied in this work is a crucial step towards building functional silicon nanowire based systems and devices.

5.3.1 Experimental Setup

The conventional synthesis process was therefore carried out in the presence of silane and a dopant source. Both p-type and n-type doping processes were attempted. For n-type doping the 10% silane gas supply was replaced by a premixed 98.4% silane and 1.6% phosphine gas supply typically used for CVD of doped polysilicon (98.4Si:1.6P). For p-type doping a 0.1% boron tetrachloride (BCl_3) in helium supply was used in conjunction with the 10% silane supply. In both cases the chamber pressure has changed, but otherwise all experimental conditions were identical to the undoped synthesis process. The chamber pressure for the n-type doping experiments was 140-150mTorr while the chamber pressure increased to approximately 475mTorr with the addition of 75sccm of the independent BCl_3 gas supply to 100sccm of the

10% SiH_4 gas supply. In the n-type case, the low pressure reflects a low flow rate as it was desired to approximately maintain the 10% silane inflow which has been effective with the undoped experiments. For the p-type doping trials, the Si:B ratio was calculated to be approximately 140:1.

5.3.2 Results

The outcome of the n-type doping attempts is seen in Figure 5.17. The n-type doping results no longer illustrate nanoscale structure dimensions; instead, microscale cylindrical wires with an average diameter measuring nearly 500nm resulted. The silane to phosphine ratio in the premixed gas supply is hypothesized to be the culprit in the loss of the desired dimensionality as it has been observed that microwires do results when the phosphine concentration is too high [85]. The 98.4Si:1.6P ratio is significantly higher than effective silicon to dopant ratios reported in the literature [37]. The increase in length scale may also be attributed to the poisoning effect of phosphine or the tendency towards accelerated grain growth [86, 87]. The large dots on the synthesis surface may indicate that the phosphorous is playing a role in the formation of the liquid alloy and or the nucleation of the reaction. A changing cross section of the wire as a function of length, or tapering, is clearly seen in these samples and is an indication of sidewall deposition during the VLS process. The unfaceted nature of the nanowires indicates that this synthesis process yielded amorphous rather than single crystal structures. The average peak growth rate within the 140-150mTorr range is 0.85μm/min significantly faster than the low pressure silane only synthesis experiments. Interestingly, the increased growth rate associated with the addition of

phosphine contradicts observations made with respect to the co-deposition of phosphine in silicon thin film doping [87, 88]. The sensitivity of the growth region to surface temperature and thus off-centered growth is apparent in these experiments as well. Along these lines, it is also observed that nanowires are rather consistently

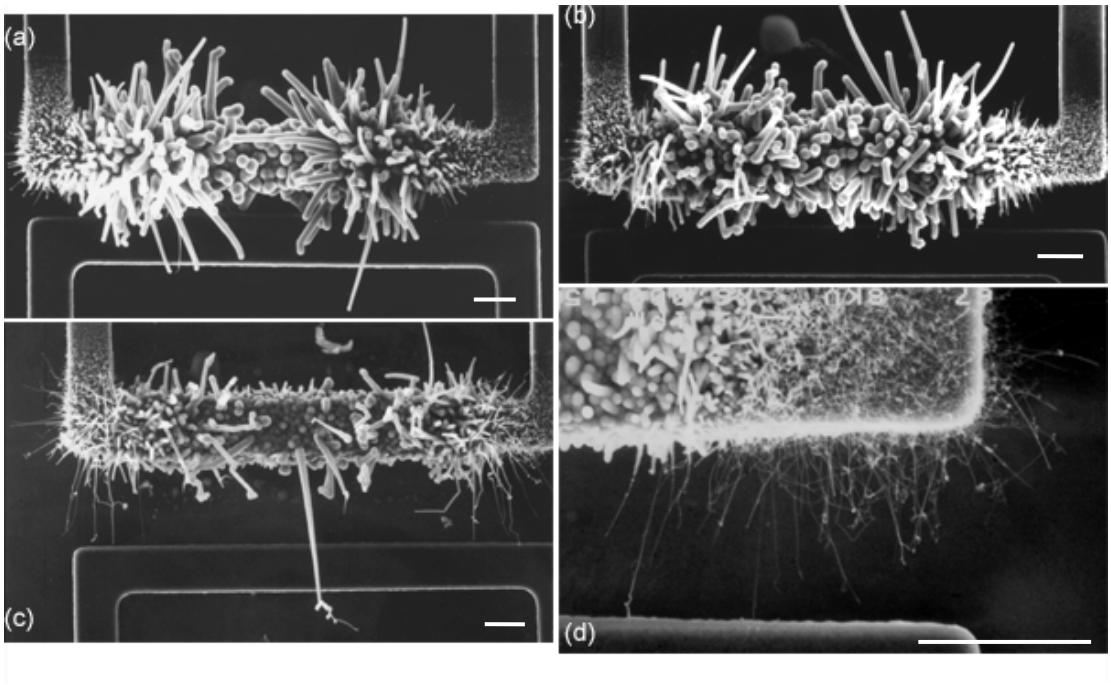

Figure 5.17. n-type in-situ synthesis doping attempts using a SiH_4-PH_3 source. (a-b) Microscale wires resulting upon the addition of phosphine to the vapor phase supply. (c-d) Evidence of 'typical' nanowire growth at off-centered, cooler regions of the growth structures suggesting that the surface temperature may have been too low for the decomposition of PH_3 resulting in a SiH_4 reaction only. (All scale bars are 5μm.)

visible at a few off-centered regions and these growth regions seem to resemble undoped results (Figure 5.17(c-d)). It could be surmised that in these regions the temperature was not sufficiently high to bring about the decomposition of phosphine, and therefore, phosphorous did not participate in the reaction resulting undoped silicon nanowires.

The p-type doping efforts are seen in Figure 5.18 and these attempts do not

appear to alter the geometry of the nanowires. In many cases or approximately 50% of the time, a semi-transparent film is visible in the vicinity of the nanowires. It is not

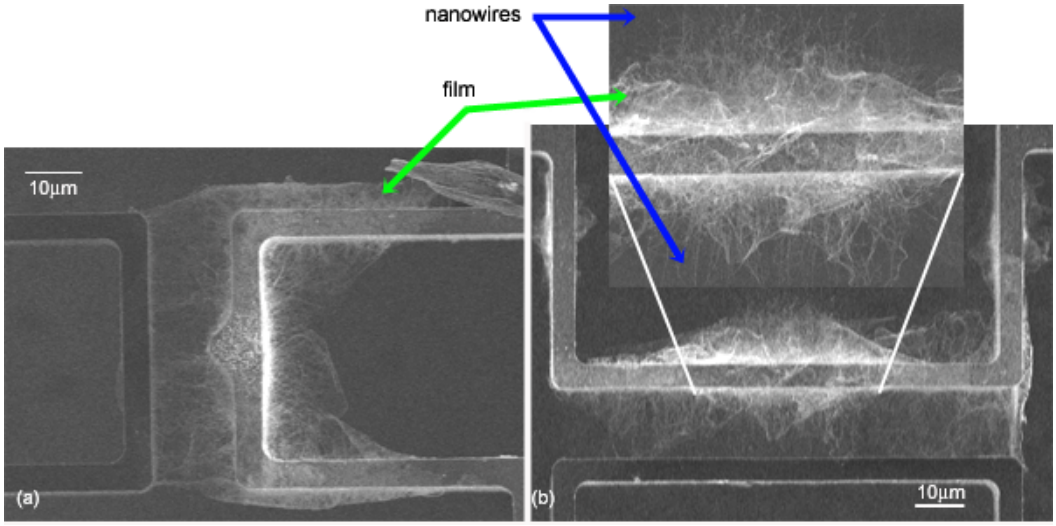

Figure 5.18. p-type doping attempts and an unidentified byproduct of the reaction. (a-b) The incorporation of a BCl_3 source often leaves behind nanowire growth along with localized coverage by an unidentified e-beam sensitive material.

known what is the composition of this material; however, it is electron-beam sensitive and often disappears after an interaction with the beam inside the SEM. The nanowire growth rate in the presence of BCl_3 is significantly reduced over the silane only synthesis process yielding an average peak growth rate of 0.33µm/min. There is some evidence in the literature that this behavior may be consistent with in-situ thin film silicon doping with a BCl_3 source [89].

Gauging the success of the doping attempts presented an additional challenge. The I-V characteristics for the p-type doping attempts do not reveal improved conductance. However, the measurements setup may mask the improved doping levels due to the high contact resistances.

5.4 The Self-Assembled System in a Proof-of-Concept Sensing Application

The resulting self-assembled system is ready for development into functional devices and applications. It is particularly attractive for sensing purposes as suspended nanowires provide increased surface area and thus increased reaction surface that should translate into improved sensitivity and response time when compared to currently available sensors. Ideally, improved performance should be noted with respect to existing nanowire-on-surface designs as well as microscale devices. In order to turn the as-synthesized system into a specific sensor, additional post-processing steps are required. Such post-processing steps serve to functionalize the system for a specific application and further contribute to enhanced understanding of how the self-assembled system reacts and interacts with its environment. For a proof-of-concept demonstration, a hydrogen sensor application is sought.

5.4.1 Hydrogen Sensing Mechanism

A chemiresistor sensing mechanism based on the interaction of specific gases in the environment with the sensing surface with to yield a recordable change in conductance is sought in this work. Highly catalytic metals are suitable for this purpose and the use of palladium for the detection of hydrogen has proven effective in thin film sensors [90-92]. The concept behind this application demonstration is based on mimicking a thin film palladium based sensor with the additional advantage of increased sensing surface area. Therefore, in the resulting configuration an evaporated thin palladium layer serves as the active element responsible for

interacting with hydrogen while the self-assembled system serves as the supporting structure and the interface to the measurement tools. The chemiresistor sensing mechanism suggests an increase in resistance upon exposure of a thin palladium layer to hydrogen gas as hydrogen adsorbed by the surface dissociates and proceeds to diffuse into the thin film thus creating scattering centers which lead to recordable changes in transport properties [91]. The increased surface area offered by this device should be its primary advantage. For example, when compared to a 1μm long and 1μm wide thin film sensor, the increase in surface area offered by a $1\mu m^2$ area outfitted with a typical nanowire region and nanowires of average diameter (45 nanowires/μm^2, 45nm diameter) is 6 fold.

5.4.2 Deposition of Thin Films onto 'As-Synthesized' System

A post synthesis thermal evaporation of approximately 200Å of palladium is used to enable the functionalization of the system for a basic hydrogen sensing application. It is interesting to note that the Pd deposition is conformal and the configuration of the self-assembled system is maintained (Figure 5.19). In fact, the nanowires assist in patterning the palladium. A significant change in the extent of nanowire curvature and bending is evident following the deposition process and is probably due to the thermal stresses introduced during the evaporation process and subsequent temperature change. The thermal coefficient of expansion of palladium is 4 times larger than that of silicon. The introduction of palladium to this system does suggest another set of considerations. For example, the functionality of the sensor

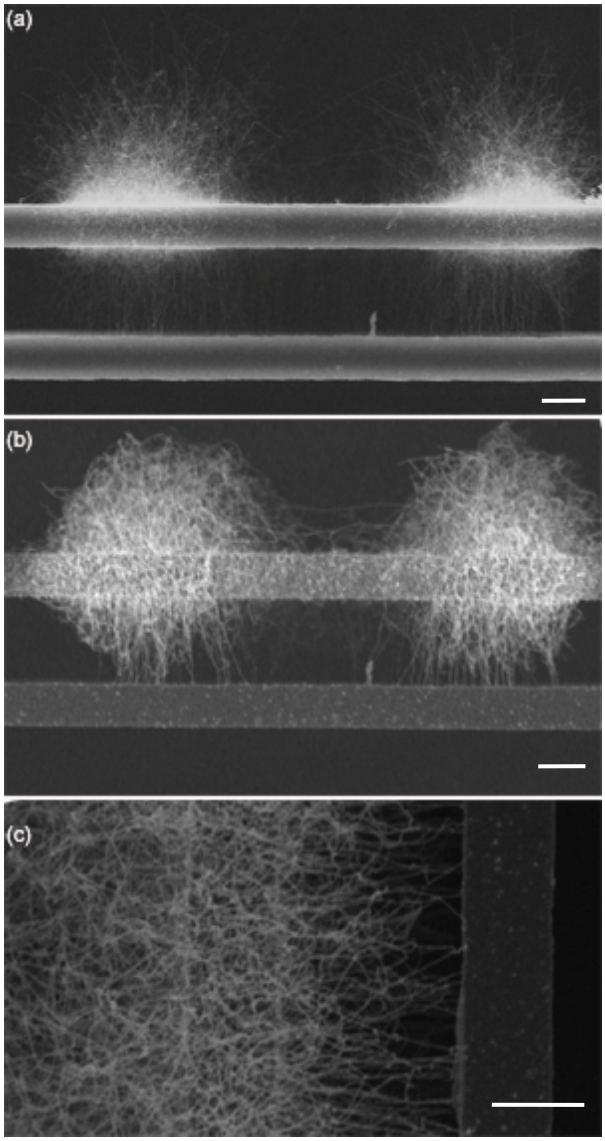

Figure 5.19. Deposition of palladium onto the as-synthesized system. (a) As-synthesized micro-to-nano system. (b) As-synthesized system following the thermal evaporation of 200Å Pd. (c) Close-up view of Pd coated silicon nanowires near growth (left) and secondary structures. (All scale bars are 5μm.)

could be compromised due to the formation of a palladium-silicon silicide (Pd_2Si), since, Pd_2Si has been shown to form as a result of palladium deposition onto a silicon surface or following annealing at as low as 200-220ºC [69, 93]. However, it is believed that in this case two distinct layers remain. The formation of a silicide is

hindered by the short evaporation time, the low sample temperature (as the sample surface briefly reached ~100ºC while the suspended nanowires remained even slightly cooler) and the presence of the native oxide that has been shown to delay silicide formation [81, 93, 94].

5.4.3 Sensor Properties, Testing & Results

The fabricated device is ideally a functional sensor; however, its performance is hindered by the low carrier concentration in the nanowires. This limitation translates

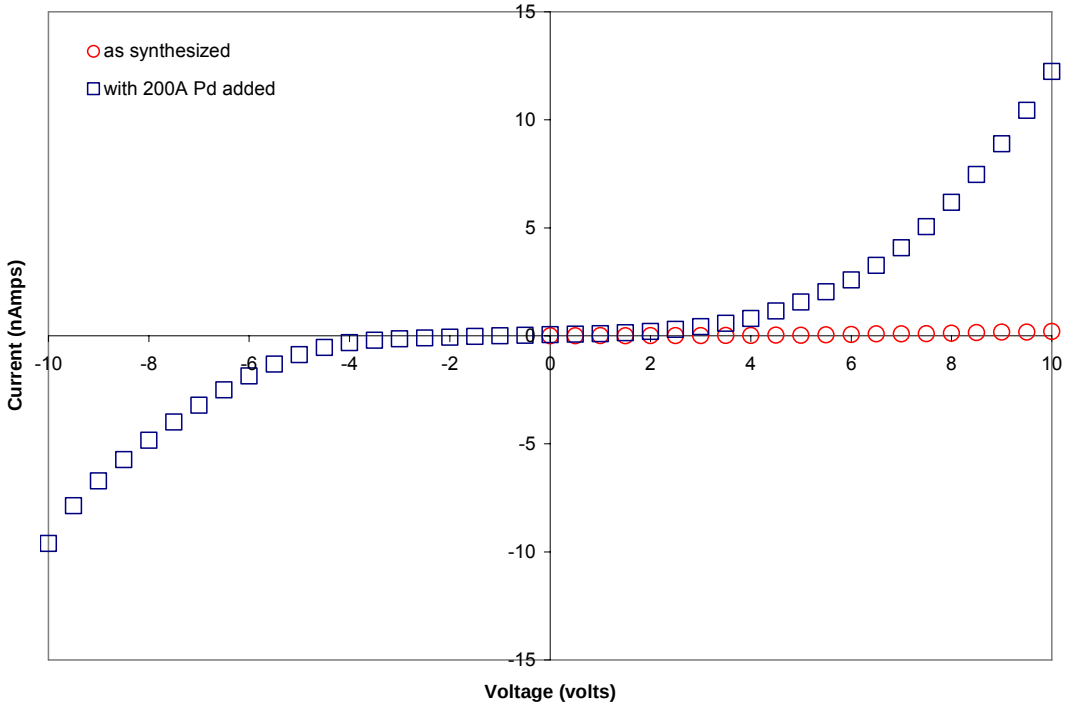

Figure 5.20. I-V characteristics following the mask-less deposition of 200Å of palladium onto the as-synthesized system. Improvements in the current carrying capacity of the system are evident, yet non-linearities still remain.

into high nanowire resistances resulting in very low current levels passing through the system as illustrated by the I-V relationship of the device seen in Figure 5.20 and

previously discussed. The I-V relationship following the palladium deposition does seem improve conductivity and suggest the formation of an additional conduction path across the device although these results do not match the values expected for a long and thin metallic interconnect, for example.

Sensor tests were conducted in a vacuum chamber, where the device was intermittently exposed to a flow of 100 PPM of hydrogen in nitrogen and no flow. The chamber pressure remained constant during these changes. In order to gauge if a change in resistance was taking place upon exposure to hydrogen and since high resistances are inherent to the system, the response was recorded using an amplifying circuit. The amplifying circuit, an Analog Device 549JH inverting operational amplifier with ultra low impedance current [95], served to both amplify the output signal and cut off high frequencies present in the surroundings. A diagram of the op-amp and circuit connections is shown in Figure 5.21, and the resistance across the nanowires was determined by correlating the gain (*Vout/Vin*) of the amplifier and the impedance resistance across the amplifier (*Rc*) as described by Equation 5-3 for low frequencies, where *Vin,* the input voltage, is set at a constant value ranging from 1 to 10V. The output voltage (*Vout*) typically recorded in these tests ranges from a few

$$\frac{Vout}{Vin} = -\frac{Rc}{Rnanowire\ array} \qquad \text{Equation 5-3}$$

millivolts to about 100mV. A typical sensor response in the form of resistance as a function of time is seen in Figure 5.22, where based on the chemiresistor sensing mechanism, an increase in resistance is expected upon exposure to hydrogen. The

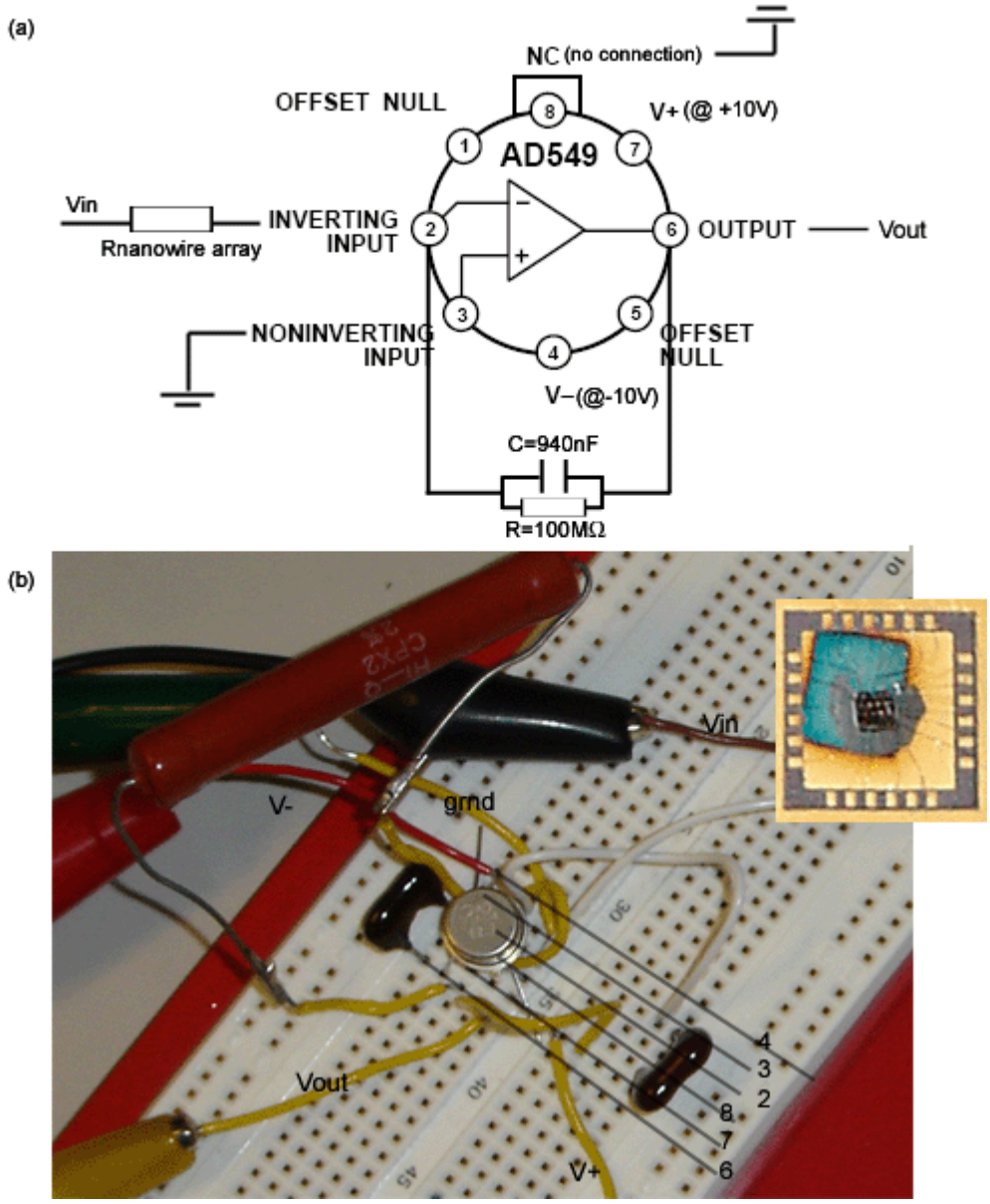

Figure 5.21. Experimental setup of the amplifying circuit for sensor testing. (a) Schematic of the circuit layout and connections. (b) Physical manifestation of schematic in (a). For illustration purposes the only the chip and its connections to bonding pads are seen, but in reality the chip carrier is mounted on the breadboard. The bluish tint on the chip carrier surface represents the extent of Pd deposition.

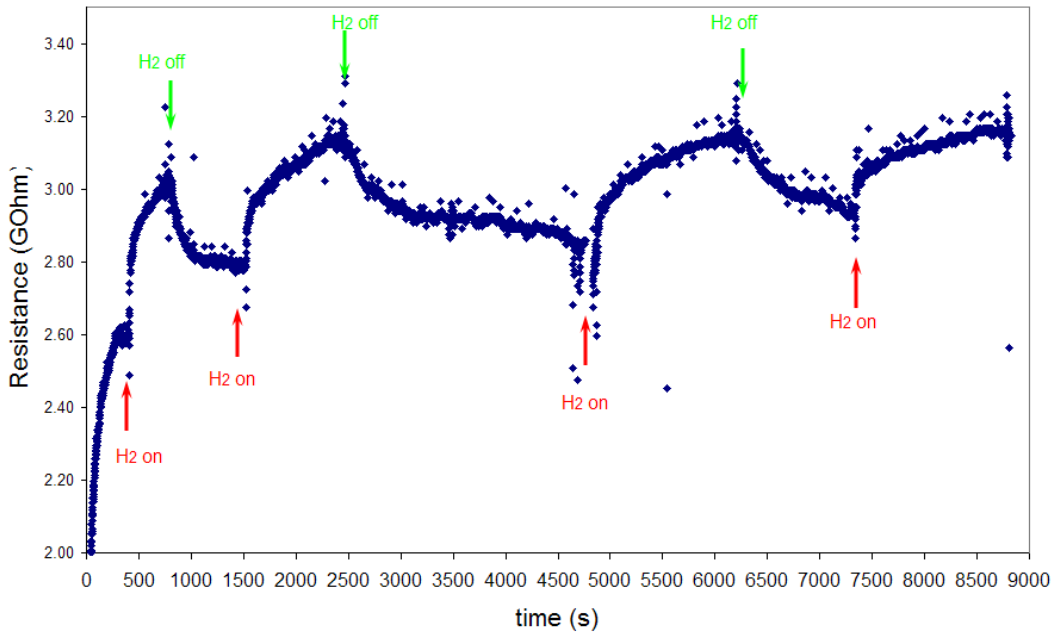

Figure 5.22. Proof-of-concept H_2 sensor response. Resistance measurements versus time illustrate an increase in resistance upon the introduction of H_2 and a decrease in resistance once the test chamber is evacuated (Vin=1V).

plot illustrates a slight yet obvious change in resistance as a function of time and hydrogen flow. The response time is slow and the shape of the curve seems to indicate a slow adsorption process [91] or possibly an inadequate sensing temperature range [96]. In addition, the sensor appears to lose sensitivity with experiment duration. To put this performance in perspective, commercially available thin film palladium based hydrogen sensors, for example, are advertised with an initial response time of 2 seconds followed by the stabilization of the signal until the environmental conditions change [92]. For the illustration of the concept, however, it is important to note the distinct trends exhibited in Figure 5.22 with and without the presence of hydrogen flow in the test chamber. It appears that the presence of

palladium is indeed responsible for the observed behavior since the response of an identical system without the additional palladium layer does not exhibit a consistent response with the introduction of hydrogen (Figure 5.23).

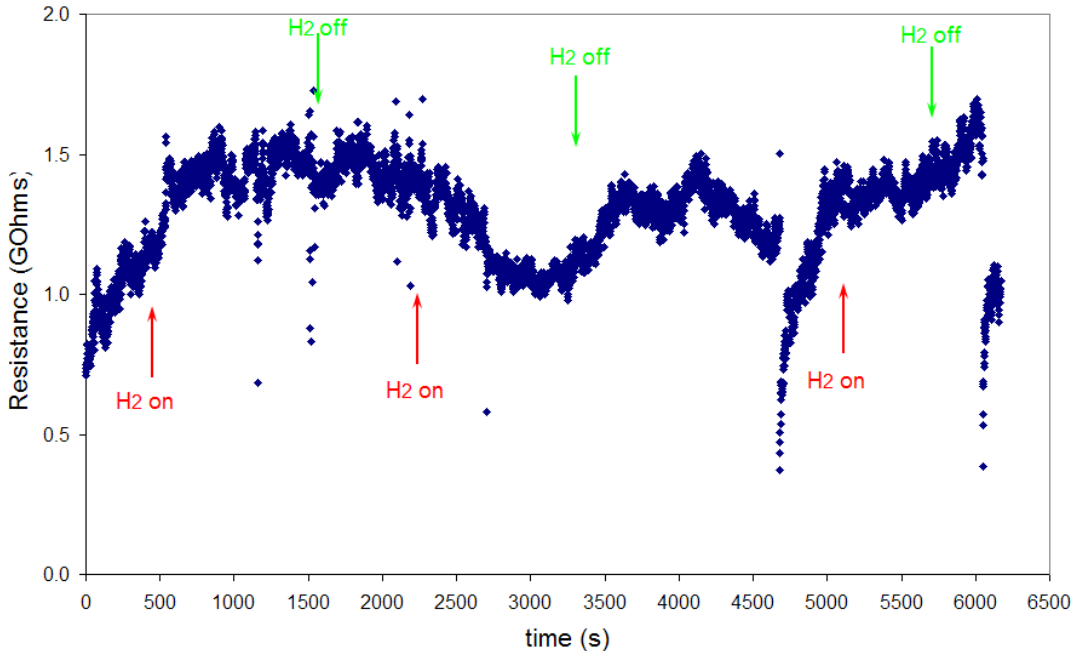

Figure 5.23. Testing of proposed sensing mechanism. The as-synthesized self-assembled system with no palladium present is subjected to alternating H_2 flow. The response does not show a well defined trend suggesting that the Pd presence plays a role in the sensing mechanism (Vin=1V).

5.4.4 Discussion

The performance of this proof-of-concept sensor, although weak, does represent a simple, basic and sought-after device application. It appears that any device application will be limited until contacts and doping issues as they pertain to the system at hand are better understood and controlled. The quality of the sensor, its response time and sensitivity are also tied to the quality of the palladium film.

However, the film thickness was intentionally minimized in order to maintain the nanowires as distinct entities and thus retain the improved surface area configuration. A better quality film may assist in improving sensor performance and in this case there is an indication that the sensor's performance may be hindered by the fouling of the palladium film due to the reaction with air or other impurities, as the response weakens with experiment time. In addition, the reversibility of the sensor and its sensitivity may be maintained by heating of the sensing surface after testing or with the introduction of a hydrogen getter to remove hydrogen present on the sensing surface. Finally, it is estimated that the conformal palladium deposition process yields coverage of approximately two-thirds of the nanowire's surface, and hence the process does not fully exploit the available sensing surface. This limitation, however, can be easily mitigated by taking advantage of the backside holes of the chip and completing both a front side and a back side palladium deposition.

5.5 Summary

The topics presented in this chapter represent key aspects of this novel approach that must be well understood and tackled before this process may be widely integrated with existing technologies. Encouragingly, the TEM analysis confirms that the localized synthesis process is indeed a result of the VLS process and further, that the localized synthesis environment does not alter the VLS process. The mechanical characterization of the self-assembled system, although mainly based on visual observation, does suggest a mechanically resilient system that can successfully withstand various post-synthesis steps. The electrical characteristics of the system are

not ideal and the difficulties here stem from two main issues: contact resistances and lack of doping. Once these issues are satisfactory addressed the system should be suitable for a variety of applications. The proof-of-concept sensor application does show the potential of the system which coupled with the ease of fabrication and assembly make for an attractive solution.

6 Conclusions & Future Work

6.1 Dissertation Summary

6.1.1 Process Capabilities

The technique developed in this work provides a simple, rapid, reliable, controllable and repeatable approach for the direct nano-to-micro integration. At the core of this integration process is the utilization of specially designed microscale structures that serve as the platform for the chemical synthesis of 1-dimensional nanostructures, permitting the in-situ nano-to-micro integration during the synthesis process. The process is unique as a localized heating process not only confines the high temperature region but also permits spatial control over nanowire placement.

The VLS growth mechanism is used in this work to enable the bottom-up, chemical synthesis of silicon nanowires. For the first time, the VLS process is pursued in local heating environment rather than the traditional global heating furnace environment. SEM and TEM examination of resulting nanowire growth regions reveals that the VLS process is not altered by the localized heating environment and the resulting nanowires show characteristics consistent with traditionally synthesized nanowires.

Simple two-terminal systems, self-assembled as silicon nanowires link together two MEMS structures, are easily achieved using this process. The as-synthesized

position of the nanowires is their final position in the resulting system, hence eliminating the need for post-synthesis manipulation and placement required under conventional integration methods. Furthermore, the application of a localized electric-field during the synthesis process has been shown to improve nanowire organization across a gap between MEMS structures. Overall, this technique provides control over both the spatial extent and the organization of the nanowires. Electrical and mechanical properties of the self-assembled system were analyzed and suggest a mechanically resilient system with low current carrying capacity due to the nature of intrinsic silicon. The ease of fabrication enabled by this technique is extremely attractive en-route to parallel, high volume integration of the nanoscale with larger scale systems. A stepwise comparison between the this technique and currently practiced integration techniques in terms of fabrication and processing needs is enumerated in Table 6-1 and reveal significant advantages of the newly suggested approach.

The process described in this work is touted as a CMOS compatible process, yet gold is an important component of the experimental setup, begging the question – how? This process is a CMOS compatible process as the integration of the silicon nanowires is a final fabrication step following all circuitry and microfabrication steps. Inline with the grand vision presented in Figure 1.2, this process enables the nano-elements of the chip (quadrant I) to be integrated late in the fabrication process, once all other components are in place. Since the synthesis and assembly processes are localized, no interference with other devices or components will occur as a result of

this integration process. Overall, this approach truly addresses a key challenge facing nanotechnology and provides an executable, simple and cost effective method.

Traditional Methods (EBL based)	Suggested Alternative
1. Synthesize nanostructures	1. Fabricate MEMS structures
2. Sonicate to remove nanostructures from substrate	2. Deposit catalyst
3. Place nanostructures in solution	3. Localized heating in presence of vapor phase reactant
4. Prepare electrode substrate w/ electron beam sensitive polymer	4. Synthesis, assembly and integration of nanostructures
5. Dispense nanostructure solution onto substrate	5. Device complete
6. Scanning Electron Microscopy to locate nanostructures	
7. Electron Beam Lithography of contacts	
8. Thermal evaporation of metal electrode	
9. Lift-off of polymer layer	
10. Device complete	

Table 6-1. Stepwise comparison of traditional EBL based integration schemes and newly suggested approach.

6.1.2 Process Improvement Opportunities

Since the goal of developing a high yield, manufacturable and economic approach for the incorporation of a burgeoning technology is at the core of this work, the limitations of this process must be addressed as well. The demonstration of this process was performed in a rather crude manner and few changes and upgrades in terms of MEMS structure properties, VLS reactants and process procedure and control could prove beneficial.

The following is a list of possible ideas; some, however, are mutually exclusive. Ensuring good quality nanowires is key when developing this process and improved nanowire quality has been shown with the use of silicon tetrachloride ($SiCl_4$)

explained by the more controlled decomposition of $SiCl_4$ when compared to SiH_4. In addition, the combination of $SiCl_4$ with H_2 as the carrier gas enables the creation of hydrochloride acid, a known oxide etchant which can help in keeping surfaces clean, a limitation of the existing process [22]. The presence of H_2 is also believed to assist in passivating surfaces, a very useful attribute in this context [30]. The more controlled decomposition of $SiCl_4$ is a function of its thermal decomposition temperature, which will require, therefore, slightly higher synthesis temperatures (800-850ºC). Along the same lines, targeting a <111> oriented single crystal silicon surface should assist in synthesizing better quality nanowires, more controlled nanowire organization and arguably a better nano-to-micro interface. On the other hand, reducing the synthesis temperature can be easily achieved by replacing the AuPd catalyst with a gold catalyst.

The experimental setup could greatly benefit from an independent pressure and flow rate controller. The data presented in this work suggests an interesting dependence on pressure, and having the ability to more accurately compare this work with others in the literature could be valuable. In addition, the resistive heating process could easily be automated to further streamline the process.

The doping efforts described in this work were limited in terms of selection of dopant, dopant to silicon ratio and characterization efforts. Since the literature does point to successful in-situ doping, more methodical experimentation and testing should be able to yield the correct combination of parameters. The main limitation in dopant selection was high toxicity of many dopant sources and the inability of the

experimental setup to suitably meet the safety requirements when handling these gases. Boron tribromide (BBr_3) may be another possible p-type dopant source, as the B-Br bond is weaker than the B-Cl bond and only slightly stronger than the B-H bond yet less toxic [97].

Electrical characterization performed in this work analyzed the system as a whole and did not evaluate the characteristics of individual components and individual interfaces of the system. While scientifically of great interest, and possibly holding significant information about the system, in practice this type of analysis proved unusually difficult. Points of difficulty included physically achieving reliable mechanical contacts between the probe and individual nanowires as well as reliable electrical contacts in the presence of the native oxide, in addition to contact resistances and high noise levels through the measurement unit. Ideally, contact resistance issues could have been eliminated using a 4 point probe test setup rather than the 2 point test, however; the realization of the physical contact once again proved to be the showstopper. It appears, however, that with additional practice and some refinements to the process this type of analysis should be possible.

Finally, the realization of a truly parallel nanowire synthesis process, although a natural continuation of this work and overall key process goal, has yet to be demonstrated. A successful batch fabrication process requires well designed and meticulously fabricated MEMS structures arrays. In other words, the MEMS structures must be interconnected such that no additional resistances are introduced into the circuit and must each feature an identical I-V response.

6.2 Future Outlook

6.2.1 A Microscale-for-Nanotechnology Approach

The direct integration of the nanostructures with larger scale systems and specifically the microscale is a practical approach when pursuing the nanoscale, transcending far beyond being solely an enabler for device assembly purposes. As nanotechnology is maturing it is important to communicate between the two length scales. The chemistry and physics heavy approach to nanoscience often neglects available engineering tools, and it is therefore important to foster a truly multidisciplinary approach. For example, the direct integration approach presented in this work provides a unique opportunity to explore the fine properties of the nanoscale. The need is considerable as commonly used macroscale characterization tools cannot accommodate nanoscale samples. By designing MEMS structures to serve as force gauges in tensile, compression, shear, and fatigue testing stages, nanomechanics and nanoreliability issues may be evaluated experimentally with the help of the microscale devices. The direct integration approach not only simplifies sample preparation and mounting requirements but also allows an evaluation of in-situ formed contacts, currently a seldom addressed subject. In this fashion, microscale systems may truly serve as an enabler for the nanoscale.

6.2.2 Final Thoughts

Process integration, a key parameter in IC and MEMS fabrication technologies, is tackled in this work with a new flavor, namely, developing a practical and feasible nano-to-micro integration process. It is widely recognized that in order to realize the

potential of nanotechnology on a commercial basis, adequate methods for interfacing with the nanoscale must be developed. The approach presented here is simple to implement and addresses many existing needs. At the same time, this dissertation presents a rather basic proof-of-concept demonstration which relies heavily on visual observations while attempts at a more quantitative description are incomplete as limited by the samples, the tools, and yet to be perfected techniques. Therefore, in order to further the value of this work, it must be further developed, streamlined and quantitatively studied.

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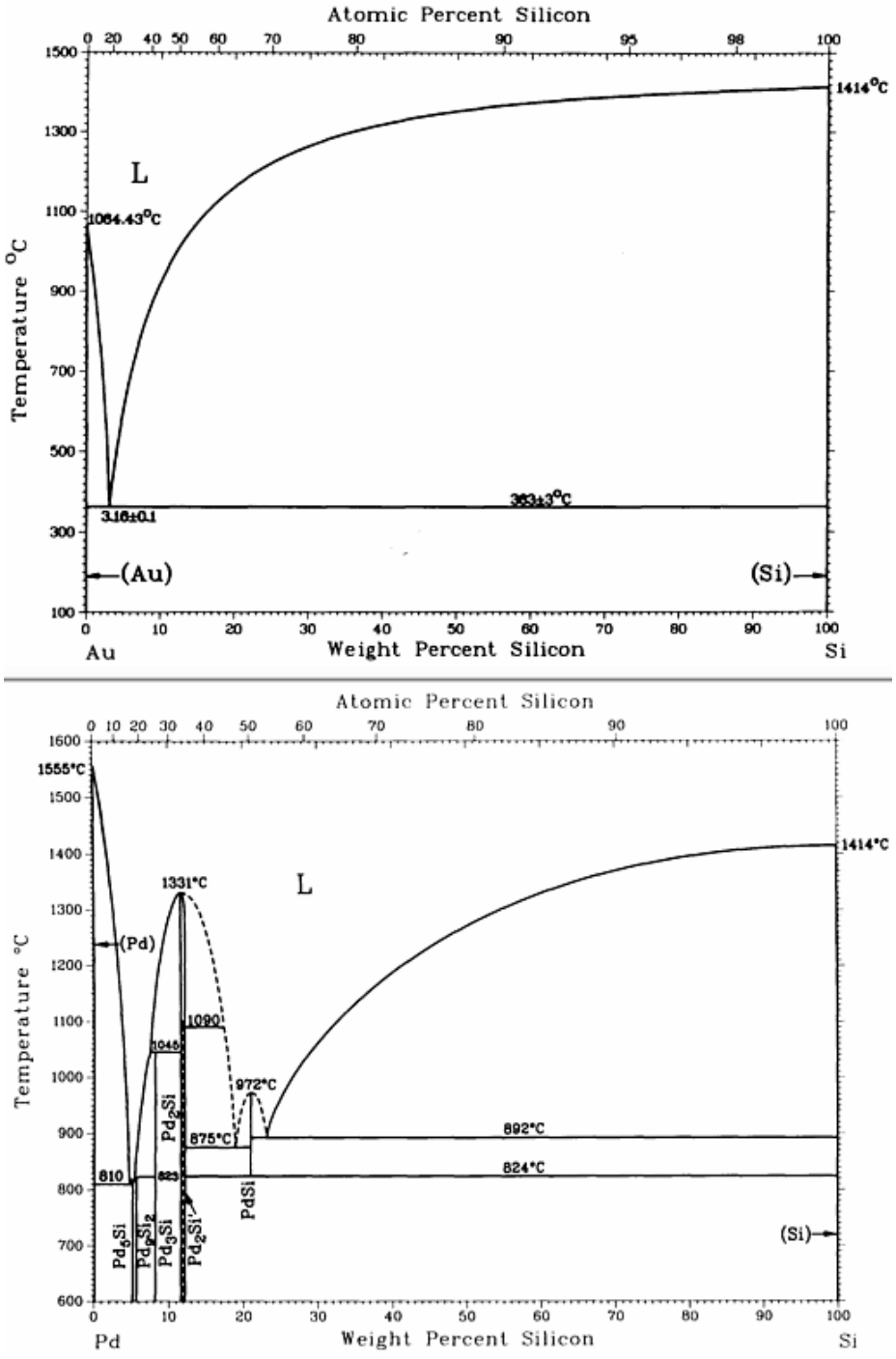
9 Appendices

9.1 MEMS Synthesis Platform Properties

	Active layer thickness (μm)	Dopant type	Resistivity (ohm-cm)	Crystal orientation
SOI/SCS				
Run #1	50 ± 1	N (P)	0.005-0.01	<111>
Run #2	50 ± 1	P (B)	0.005-0.02	<100>
Run #3-1	2 ± 1	N (As)	0.001-0.004	<100>
Run #3-2	15 ± 1	P (B)	0.006-0.01	<100>
Poly-MUMPs	(poly1)			
Runs 15, 57,65	2 ± .03	N (P)	0.0018-0.0023	-----
Poly-Si				
Run #1	2	N(P)	0.03-0.06	-----

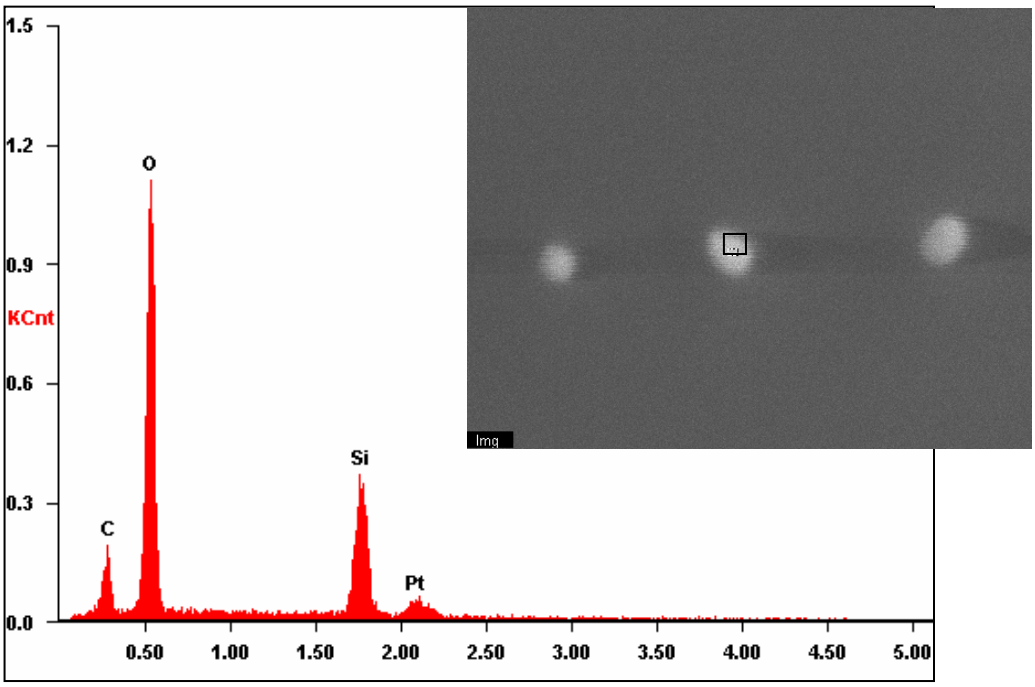
9.2 Binary Phase Diagrams

Gold-silicon & palladium-silicon binary phase diagrams [98].



9.3 Localized Metal Deposition Attributes

EDX Spectrum taken on Pt deposition site



EDX Spectrum taken away from Pt deposition site (location marked by box)